Selective isotropic etching of Group IV semiconductors to enable gate all around device architectures

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Chemical Oxide Removal (COR) Reaction Mechanism: Case for SiO₂ etch

- HF and NH₃ adsorb on the SiO₂ surface, reacting to form (NH₄)₂SiF₆ (Ammonium Fluorosilicate - AFS)

Slide courtesy: Tokyo Technology Solutions
A typical oxide etch process with Certas

~4X Volume Expansion
12nm Oxide Removal Recipe

(COR → PHT) process can be repeated in cyclic fashion to meet process requirements

Ability to:
- Process with PR
- Additional knob to control:
  - Pattern wiggling
  - Pattern damage

Slide courtesy: Tokyo Technology Solutions
Nanosheet Selective Etches

INNER SPACER MODULE

HM: SiN (or SiCN, SiOC)
Spacer: SiOxCyNz
Inner spacer: SiOxCyNz (would be different from spacer material)

Spacer formation
Fin recess
Cavity etch
Inner spacer formation
Nanosheet Selective Etches

SD/ILD0/RMG MODULES

N-EPI: SiGe:B, P-EPI: Si:P
CESL: SiN
ILD0: SiO2
Dummy poly (dummy gate): a-Si
Selective SiGe etch for Nanowire

Partial release:
- SiGe etch = 5-6 nm (each side, total = 10-12 nm)
- Si loss < 1 nm
- Etch target and uniformity > 5 Å
- Square SiGe etch front

Full release:
- SiGe etch ~ 25 nm (each side, total ~ 25 nm)
- Si loss < 1 nm

The above data is on blanket films
Summary for Si/SiGe stack:

- Selective SiGe: Si etch on imec wafer looks good (SiGe:Si >50:1)
- SiGe etch front looks VERY flat/square
- SiGe EA proportional etch time, without additional Si loss
- Partial SiGe etch uniformity ~3nm for Left /right side & top/bottom layers (incoming tapper may contribute)
## COR SiGe:Si etch: pressure optimization

<table>
<thead>
<tr>
<th>Incoming</th>
<th>POST TEL gas phase etch (Recipe B: medium etch)</th>
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</thead>
<tbody>
<tr>
<td>No process</td>
<td>P1</td>
</tr>
</tbody>
</table>

### Summary for Si/SiGe stack:

- Selective SiGe: Si etch on imec wafer looks good (SiGe:Si >50:1)
- SiGe etch front looks VERY flat/square
- SiGe EA proportional etch time, without additional Si loss
- Pressure (i.e. etch gas partial pressure) is contributing to slower etch rate due to byproduct formation depending on CD → causing left-right and top-bottom non uniformity
**COR SiGe:Si etch: “cavity” and “channel release”**

<table>
<thead>
<tr>
<th></th>
<th>Incoming</th>
<th>POST Etch</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>ET/cyc</strong></td>
<td>No process</td>
<td>Cavity etch</td>
</tr>
<tr>
<td><strong>Non-Tilted</strong></td>
<td>[Image]</td>
<td>[Image]</td>
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<tr>
<td><strong>Ge% for SiGe = 20%</strong></td>
<td>[Image]</td>
<td>[Image]</td>
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<tr>
<td><strong>Overlay comparison with incoming</strong></td>
<td>[Image]</td>
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<tr>
<td><strong>Tilted</strong></td>
<td>[Image]</td>
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</tbody>
</table>

**Summary:**
- SiGe: Si etch selectivity > 50:1
- No SiN HM loss
- ER = 70nm/min
- SiGe etch front is square

Data based on alternate test structures
### COR SiGe:Si etch: annealing effect

<table>
<thead>
<tr>
<th></th>
<th>Incoming</th>
<th>POST etch</th>
</tr>
</thead>
<tbody>
<tr>
<td>no process</td>
<td>Without</td>
<td>WITH</td>
</tr>
<tr>
<td>Non-Tilted</td>
<td></td>
<td>anneal</td>
</tr>
</tbody>
</table>

**Ge% for SiGe = 20%**

1. Steam anneal 500C 2hrs
2. RTP 850C 1min
3. RTP 850C 5s

#### Summary:
- Anneal affects the SiGe ER significantly
- Anneal also reduces the SiGe:Si selectivity at the SiGe-Si interface →
  - resulting in Si loss
  - meniscus etch front

Data based on alternate test structures
Selective Si etch for Nanowire application

Partial release:
- Si etch = 5-6 nm (each side, total = 10-12 nm)
- SiGe loss < 1 nm
- Etch target and uniformity > 5 A
- Square SiGe etch front

Full release:
- Si etch ~ 25 nm (each side, total ~ 25 nm)
- SiGe loss < 1 nm

The above data is on blanket films
# COR Si:SiGe etch: etch time optimization

<table>
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<tr>
<th>ET/cyc</th>
<th>Incoming</th>
<th>POST Etch</th>
</tr>
</thead>
<tbody>
<tr>
<td>No process</td>
<td></td>
<td>90S</td>
</tr>
<tr>
<td>Non-Tilted</td>
<td>[Image]</td>
<td>[Image]</td>
</tr>
<tr>
<td>Ge% for SiGe = 20%</td>
<td></td>
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<tr>
<td>Tilted</td>
<td>[Image]</td>
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</tbody>
</table>

**Summary:**
- **Si: SiGe etch selectivity > 10:1**
- No SiN HM loss
- ER = 7nm/min
- Si etch front is required further improvement
- Post etch surface is smooth
COR SiN spacer etch

Selective SiN spacer etch:
- Required SiN:Si etch selectivity > 25:1 (no Si loss)
- Required SiN:SiGe etch selectivity > 25:1 (no SiGe loss)

Summary:
- **SiN**: SiGe/Si etch selectivity > 50:1
- No Si loss
- SiN still preserved on SiGe layers
COR Selective dummy poly (a-Si) pull

 Dummy poly removal:
• Extremely selective Si etch ~100-200nm
• No SiN loss or SiO2 loss

Device structure

Test structure
Nanosheet Selective Etches: Updated

**Step 1**: Spacer formation

**Step 2**: Fin recess

**Step 3**: Cavity etch

**Step 4**: Inner spacer formation

**Step 5**: SD EPI

**Step 6**: CESL/ILD0

**Step 7**: Dummy poly/OX removal

**Step 8**: Channel release

**Step 9**: HKMG

Fin recess

Cavity etch

Inner spacer formation

Dummy poly removal

Test structure

Channel release
Conclusion

- **Dry plasma free** etches are advantageous & crucial for Nanowire/CFET integrations applications, due to:
  - High etch selectivity, inherent from the etch mechanism
  - No plasma damage
  - Aspect ratio dependency
  - Cyclic process (potential self limiting capability)