RMG WET PROCESS CHALLENGES AND THE PATTERNING KNOBS TOWARDS N5 AND BEYOND LOGIC DEVICES

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OUTLINE

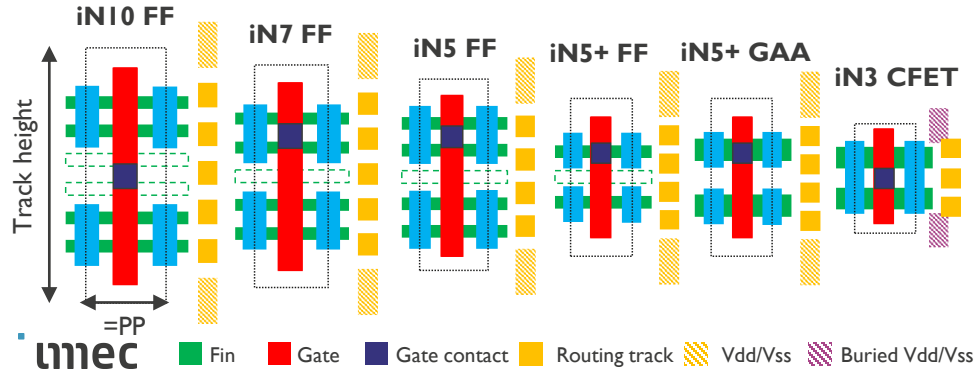
- Introduction
  - imec view of logic roadmap
  - RMG scaling challenges
- RMG patterning development
  - Tri-layer patterning scheme
  - Digital wet etching of polycrystalline metal films
- RMG scaling and multi-Vt patterning knobs
  - D&GR
  - SiH_4 soak
  - “blocked” patterning
- Summary

INTRODUCTION

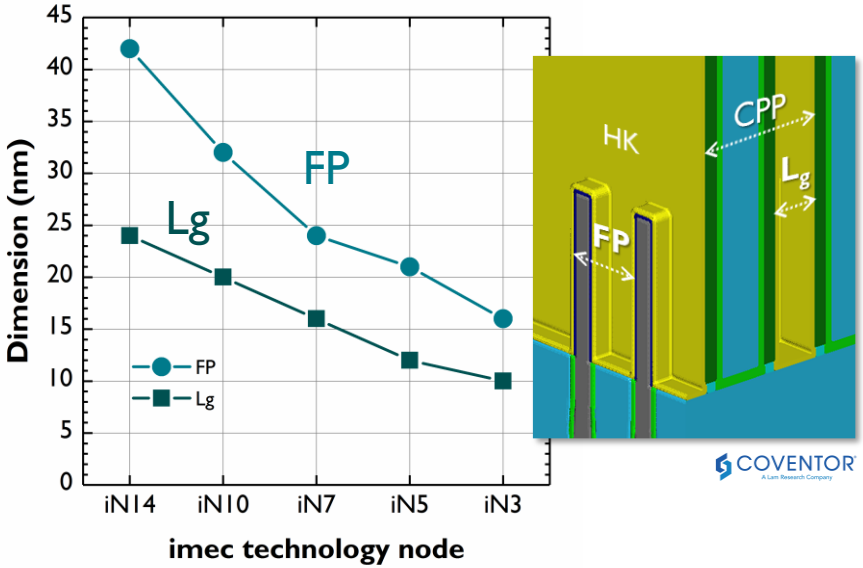
IMEC VIEW OF LOGIC ROADMAP

STANDARD CELL & REPLACEMENT METAL GATE (RMG) SCALING

"i"N: imec node	iN10	iN7	iN5	iN3
Device	FF	FF	FF/GAA	FF/GAA/CFET
Channel	Si	Si	Si/SiGe	Si/SiGe
PP (poly pitch)	56	42	42	36-42
Track height	7.5/6.5	7.5/6.5	5.5/4.5	4.X/3.X
FP (fin pitch)	32	24	21	16-21
Lg (gate length)	20	16	12	10-12
MP (metal pitch)	40	32	21	16-21



- Aggressive FP/Lg reduction needed
  - Continuous std. cell scaling
  - Device performance boost

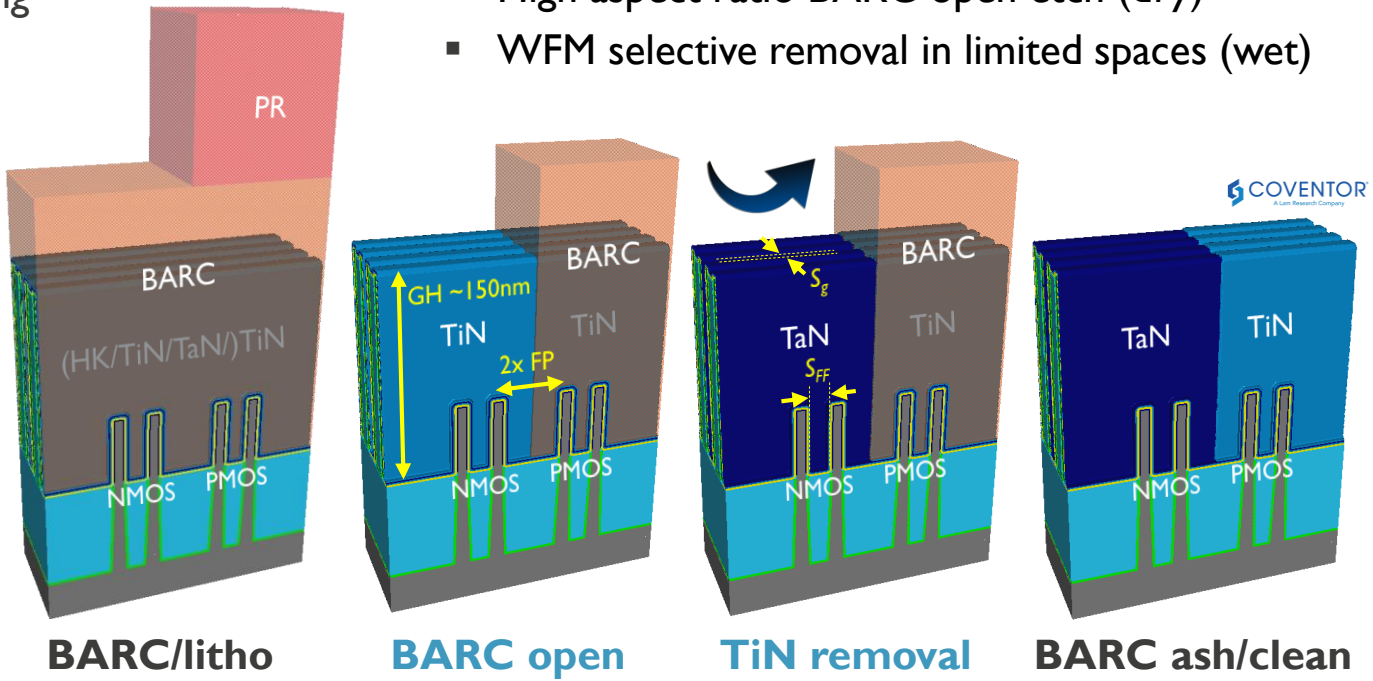


TYPICAL RMG PATTERNING SCHEME

BARC PATTERNING (DRY) + METAL REMOVAL (WET)

- Dummy poly removal
- Core/IO oxide patterning (IL formation)
- HK deposition (HfO_2)
- HK cap dep (TiN)
- Si-cap anneal (SSA)
- Barrier dep (TaN)
- **pWFM patterning**
- nWFM patterning
- W CMP

- Major challenges:
  - High aspect ratio BARC open etch (dry)
  - WFM selective removal in limited spaces (wet)



BARC/litho **BARC open** **TiN removal** **BARC ash/clean**

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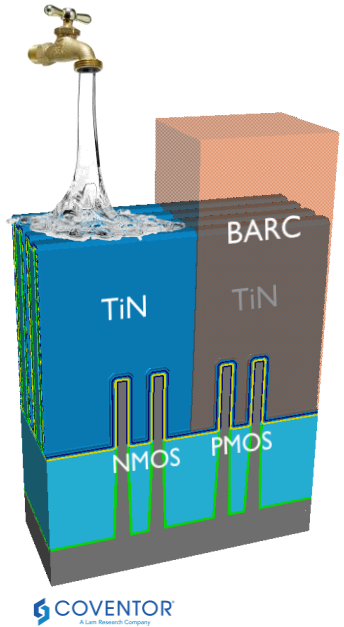
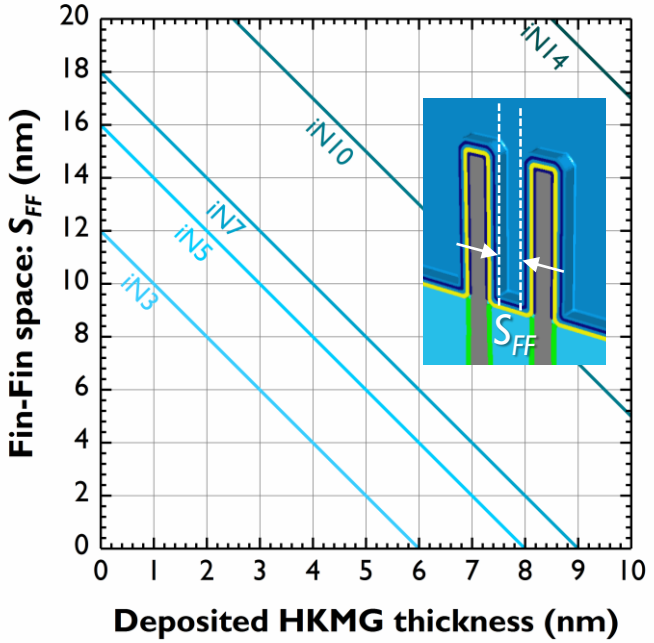
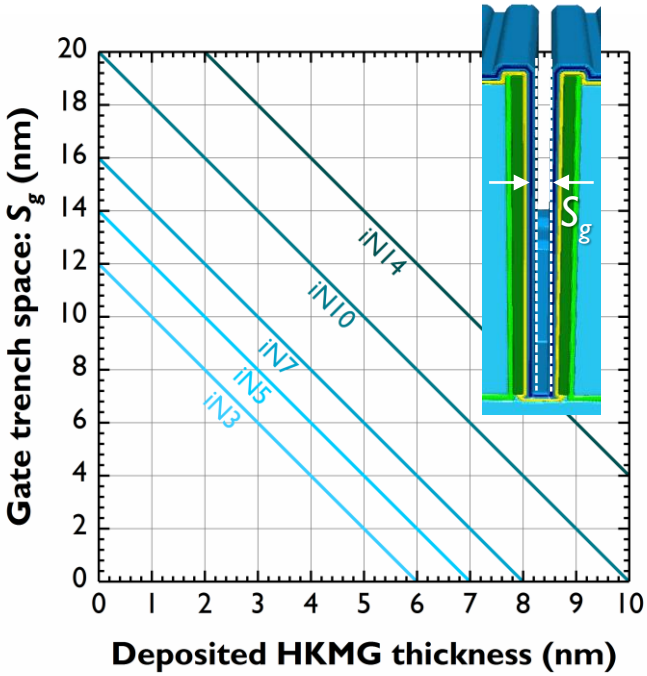
RMG PATTERNING CHALLENGES

PATTERNING SPACE

- Limited spaces for filling and dry/wet etching, cleaning, rinsing and drying
  - MG thickness reduction, eWF tuning knobs, novel patterning and optimized unit process needed







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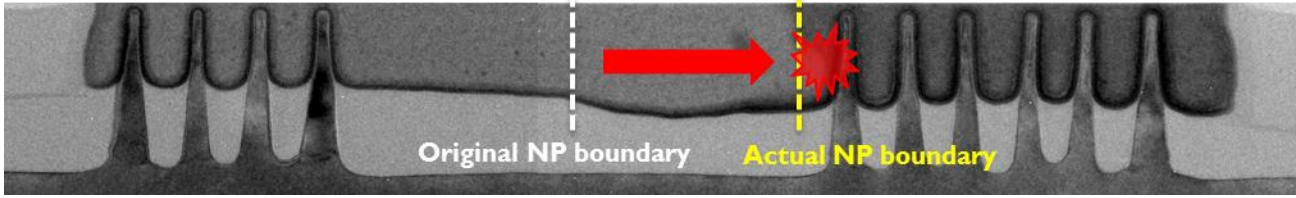
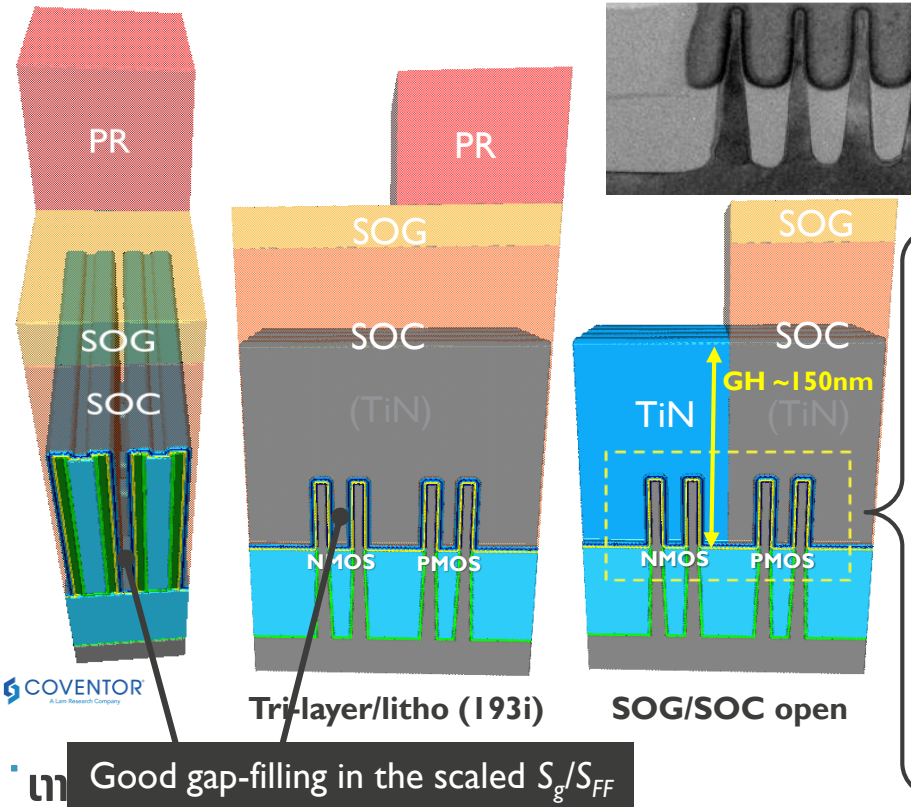
RMG PATTERNING DEVELOPMENT

* T. Hopf (imec), SPIE 2017

RMG TRI-LAYER PATTERNING
N/P BOUNDARY LATERAL ETCH

- Tri-layer e.g. PR/SOG/SOC* as the patterning mask
  - Better gap-fill capability
  - To minimize N/P boundary lateral etch

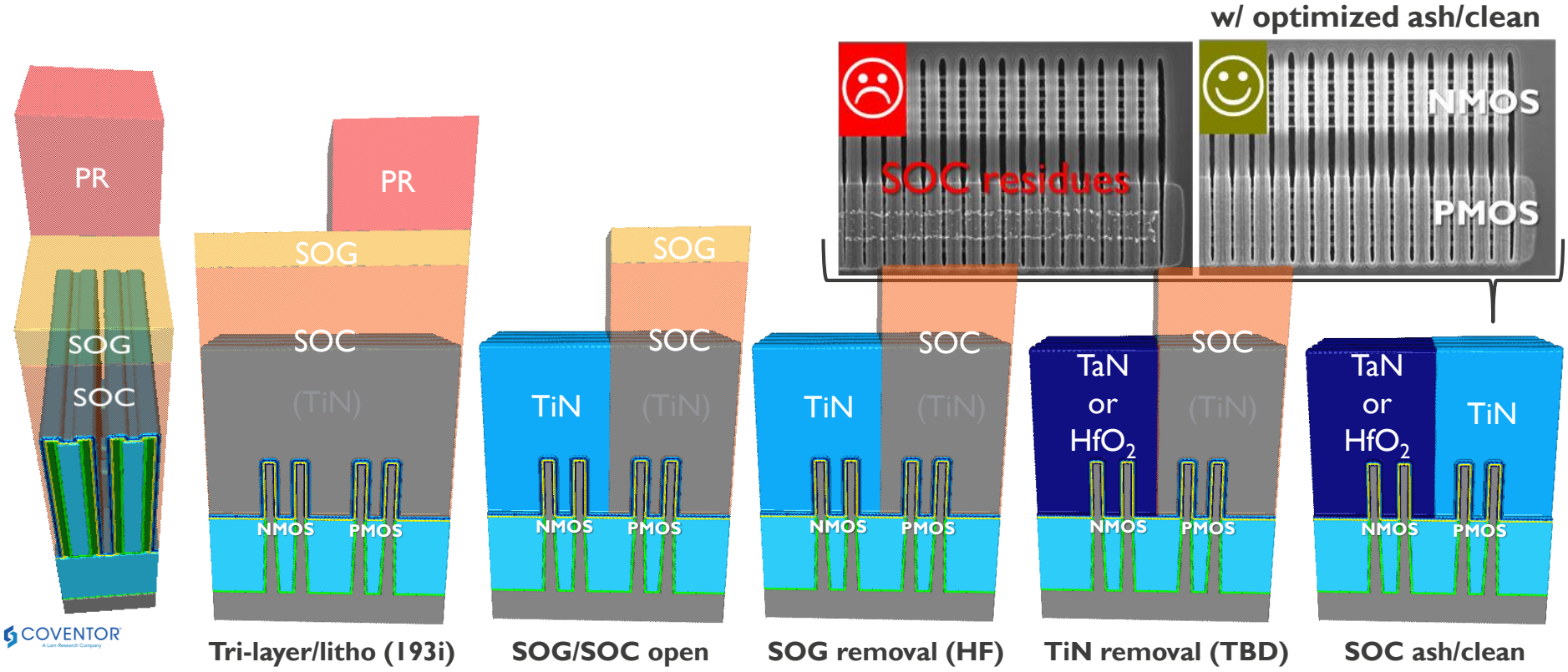




RMG TRI-LAYER PATTERNING

POST SOC ASH CLEAN

- Need to optimize SOC ash/clean



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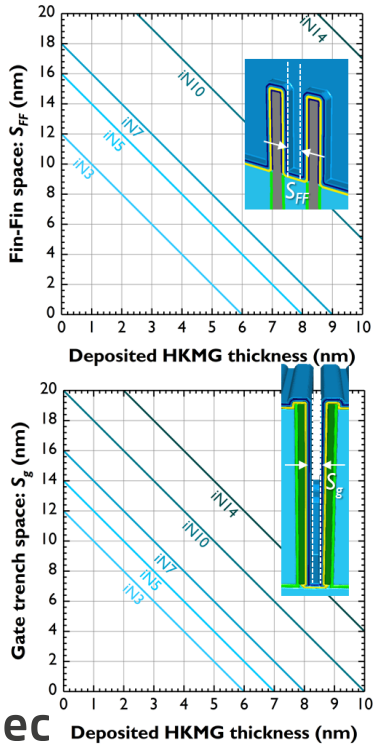
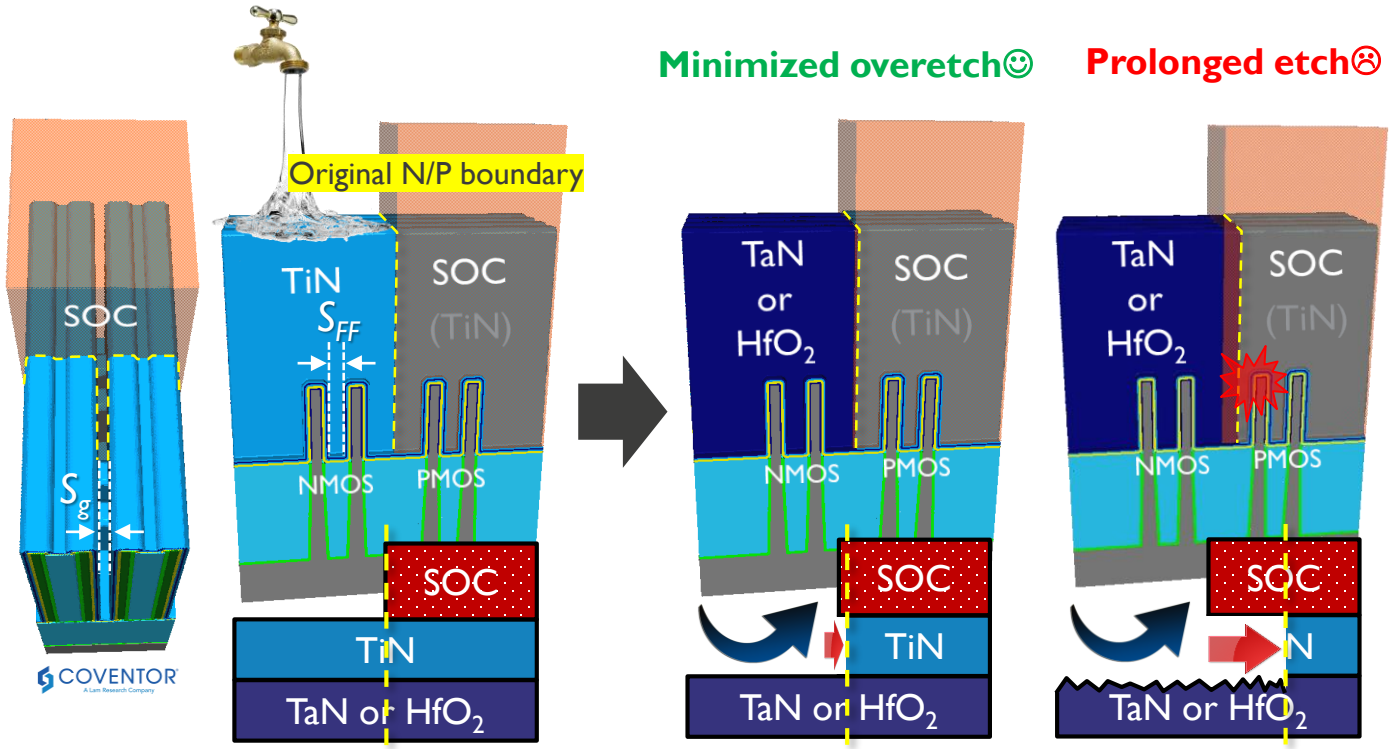
WFM WET SELECTIVE ETCH

N/P BOUNDARY UNDERCUT

- Wet etch through the limited spaces (S_{FF}/S_g) may need prolonged process
  - Prolonged wet etch will induce N/P boundary undercut and damage HKMG material underneath





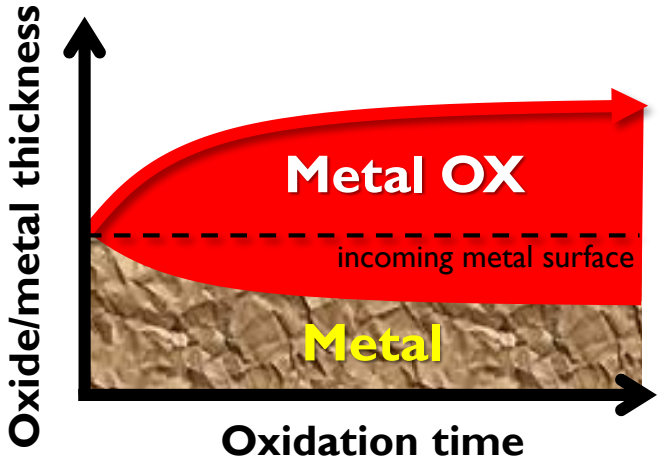
DIGITAL WET ETCHING OF POLY CRYSTALLINE METAL FILMS

CONCEPT

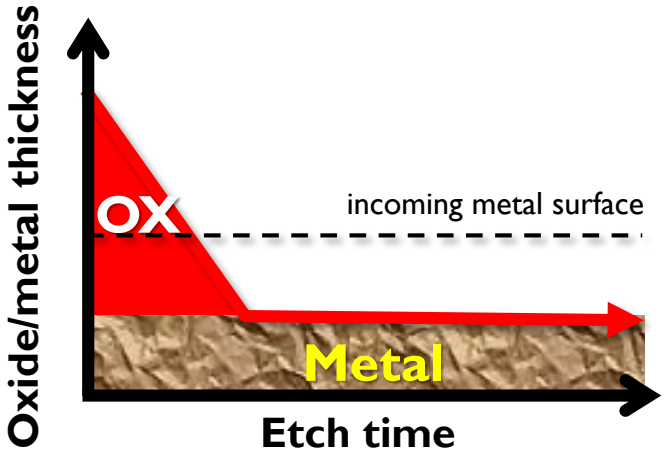
- Two-step self-limiting process
  - 1. self-saturating metal oxide growth
  - 2. highly selective oxide removal

Ref. digital etch of semiconductors:
III-V G. C. DeSalvo, JES 1996
Si T. Hattori, JES 1998
III-V J. Lin, IEEE EDL 2014
III-V D. H. van Dorp, ECS JSSST 2015

1. Self-limiting oxide growth



2. Highly selective oxide removal



- The ER determined by the formed OX thickness and etch cycle#

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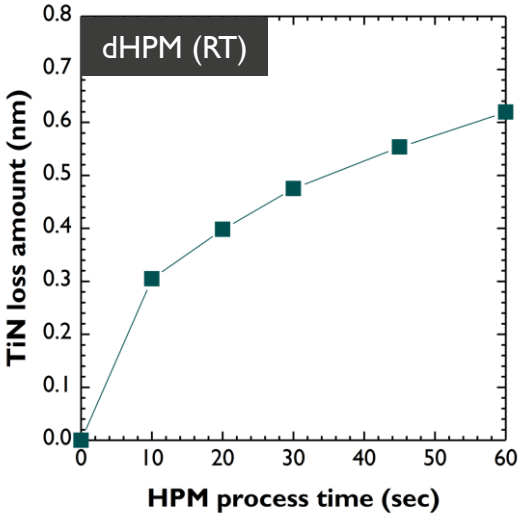
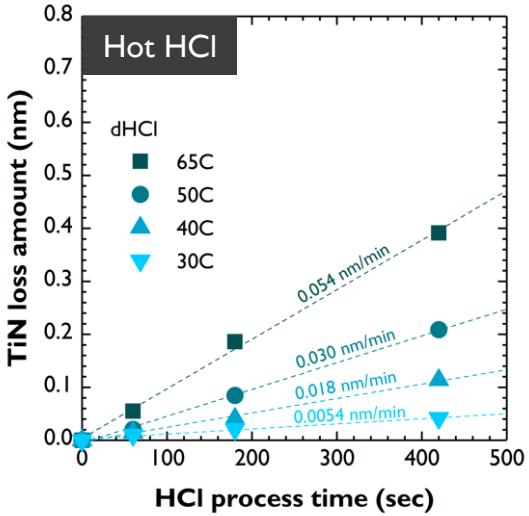
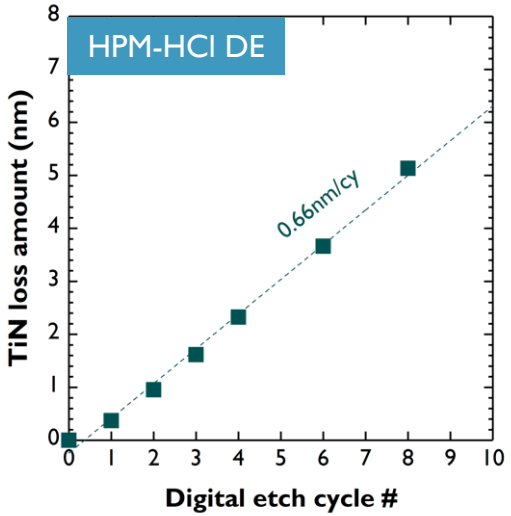
DIGITAL ETCHING OF TIN

FEASIBILITY

- dHPM (RT): self-limiting TiN etch (= self-limiting oxide growth)
- dHCl (HT): negligible TiN loss
- → HPM-HCl cycle: digital etching of TiN demonstrated (~0.66nm/cy)





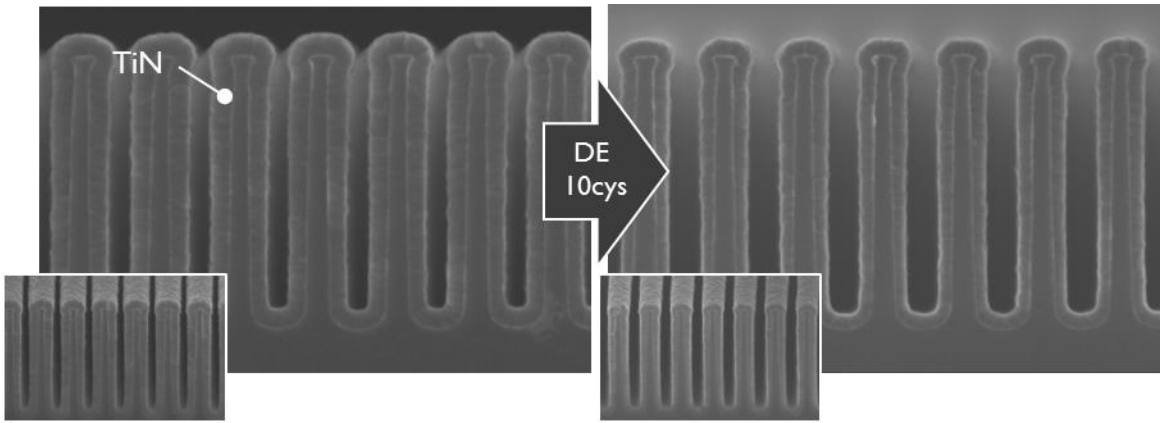


DIGITAL ETCHING OF TIN

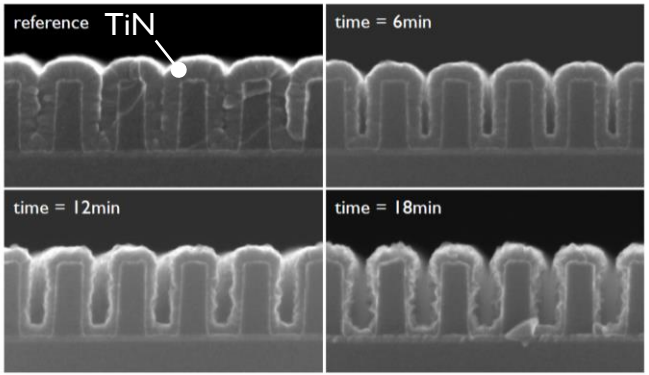
TIN TRENCH STRUCTURE

- Digital etch (HPM-HCl)
  - Conformal and uniform TiN etch demonstrated
  - Less sensitive to the TiN grain boundaries
- Ref. one-step etch (APM)
  - TiN surface roughening seen

Digital etch (HPM-HCl cycle)



One-step etch (APM)



G. Vereecke (imec), SPCC 2017

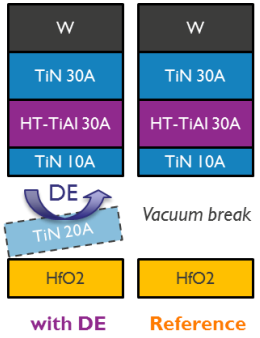
IMPACT ON ELECTRICAL PROPERTIES (MOSCAP)

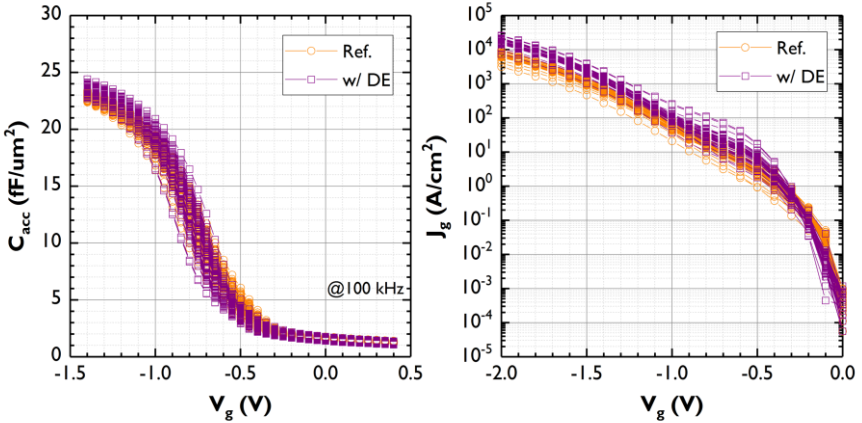
DIGITAL ETCH (HPM-HCL CYCLE) OF TIN ON HK AND TAN

TiN DE: 5cys HPM-HCl DE **on HfO_2**

- STI patterning / channel doping
- ChemOX-IL (imec clean)
- ALD-HfO2 (1.5nm)
- ALD-TiN (2nm)
- TiN removal: 5cys HPM-HCl DE
- ALD-TiN(1nm)/TiAl(3nm)/TiN(3nm)
- CVD-W
- Gate etch

Ref.

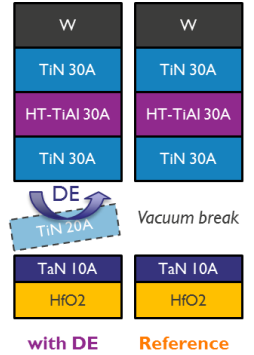


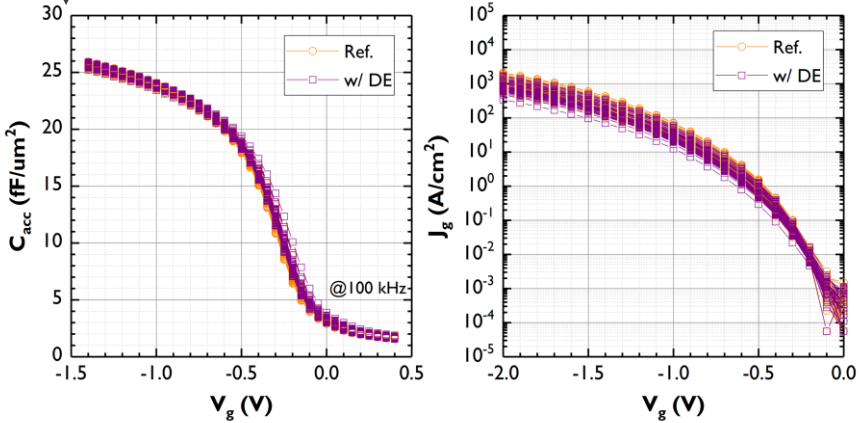


TiN DE: 5cys HPM-HCl DE **on TaN**

- STI patterning / channel doping
- ChemOX-IL (imec clean)
- ALD-HfO2 (1.5nm)
- ALD-TaN (1nm)
- ALD-TiN (2nm)
- TiN removal: 5cys HPM-HCl DE
- ALD-TiN(1nm)/TiAl(3nm)/TiN(3nm)
- CVD-W
- Gate etch

Ref.



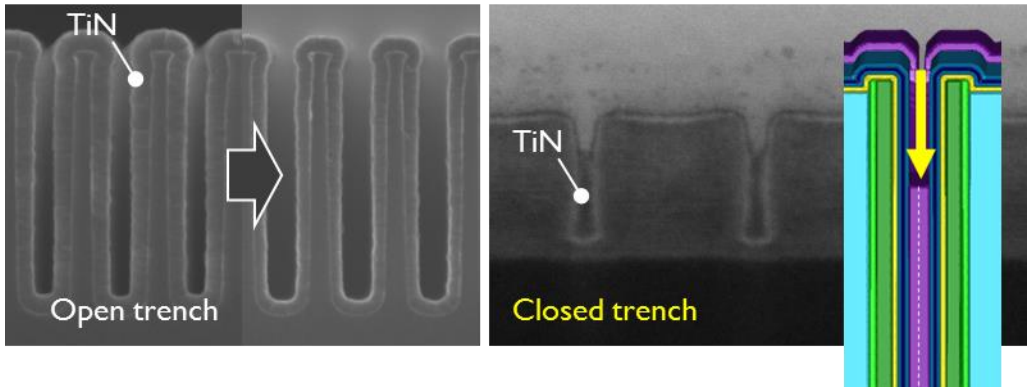


- No negative impact on electrical properties (CET, Vfb, Jg, ...) observed

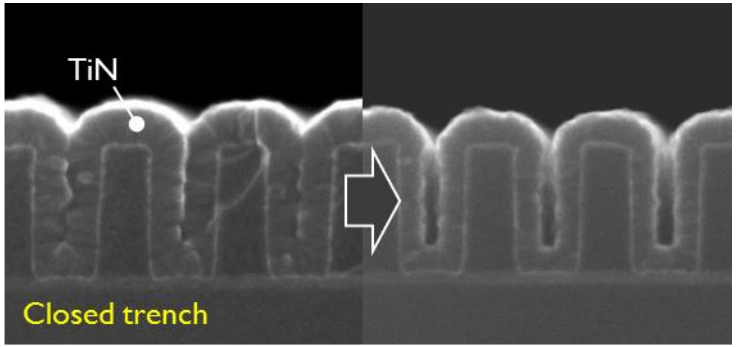
TIN DIGITAL ETCHING
CONFORMAL VS. PLUG ETCH

- Digital wet etching seems to be less sensitive to the grain boundaries and metal seam
  - Open trench → conformal etching
  - Closed trench → plug etching
  - enables metal recess etching

Digital etch (HPM-HCl)



One-step etch (APM)



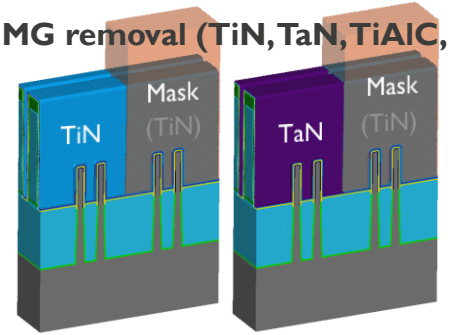
APPLICATIONS

DIGITAL WET ETCHING METAL FILMS

Selective metal removal

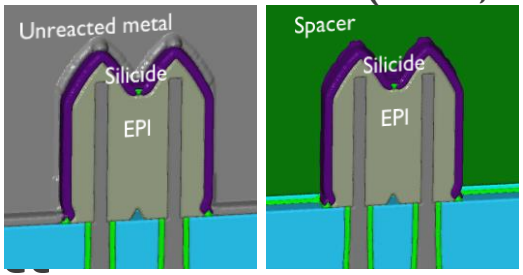
Replacement metal gate (RMG)

MG removal (TiN, TaN, TiAlC, ...)



Replacement metal contact (RMC) + wrap-around silicide / dual silicide

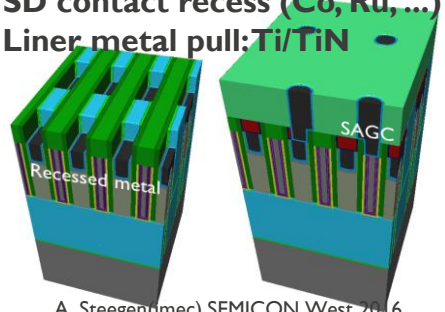
Unreacted metal removal (TiN/Ti, Ni, ...)



Controlled metal recess

Self-aligned gate contact (SAGC)

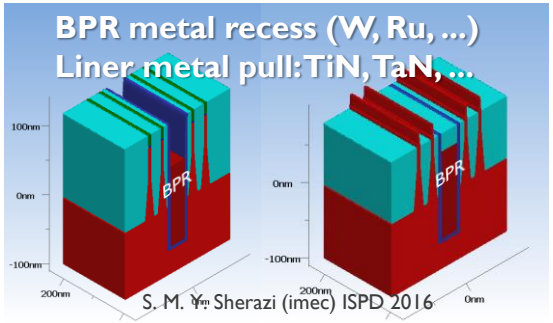
SD contact recess (Co, Ru, ...)
Liner metal pull: Ti/TiN



A. Steegen (imec) SEMICON West 2016

Buried power rail (BPR)

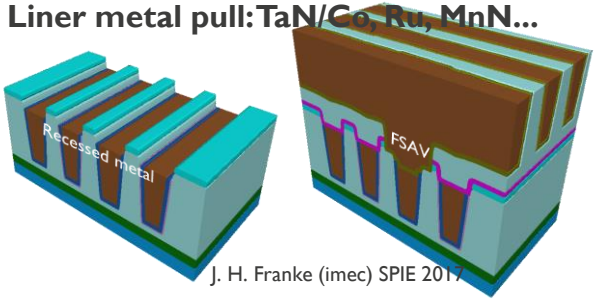
BPR metal recess (W, Ru, ...)
Liner metal pull: TiN, TaN, ...



S. M. Y. Sherazi (imec) ISPD 2016

Fully self-aligned via (FSAV)

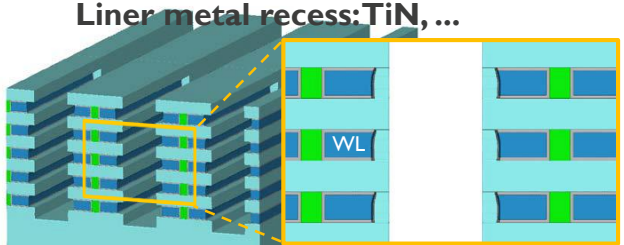
Mx metal recess (Cu, Co, Ru, ...)
Liner metal pull: TaN/Co, Ru, MnN...



J. H. Franke (imec) SPIE 2017

3D NAND/SCM

WL metal recess (W, Co, Ru, ...)
Liner metal recess: TiN, ...



L.D. Piazza (imec) SEMICON Korea 2018

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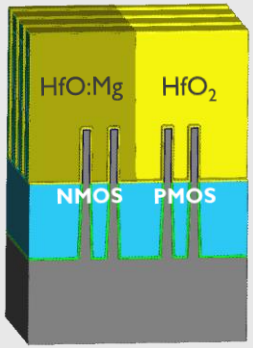
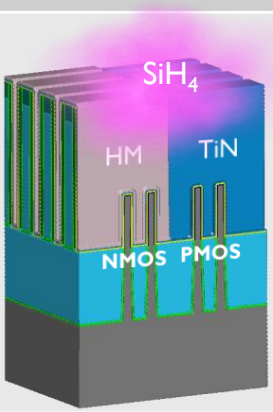
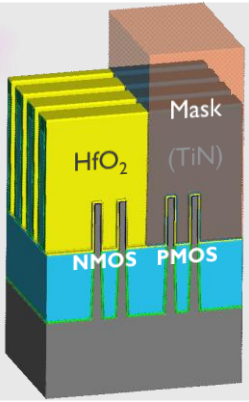
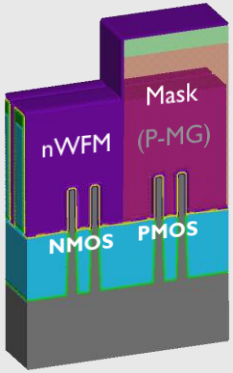
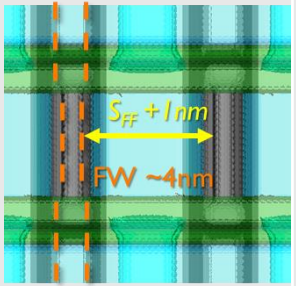
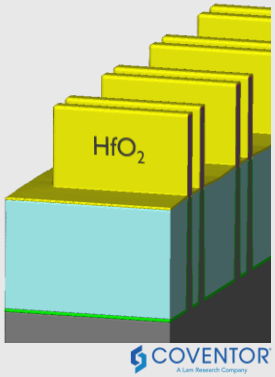
RMG SCALING & MULTI-V_T PATTERNING KNOBS

RMG SCALING & MULTI-V_T PATTERNING KNOBS

Knobs	① D&GR	② SiH_4 soak	TiN patterning on HK	③ nWFM blocked patterning	Fin CD trim in RMG	HK 1st or HKMG 1st
	Dipole	O scavenging	Skip TaN barrier	CMP assisted RMG patterning	Improve electrostatic w/o R_{ext} penalty	Go back to old tech.
						
Pros	Volumeless V_t tuning	Zero-thick V_t tuning	~2nm S_{FF}/S_g gain	Allow merged nWFM	~1nm S_{FF} gain	HKF: ~3nm S_g gain HKMGF: no S_g limit
Cons	Corrosive materials Patterning difficulty HM thickness scaling Post dry etch residue	HM thickness scaling SC/LC loading?	HK exposure/damage IL regrowth nWFM Al diffusion	Process complexity	I/O compatibility No S_g gain	FEOL metal contam Low thermal budget HKMG rem. bf. SD GAA incompatibility

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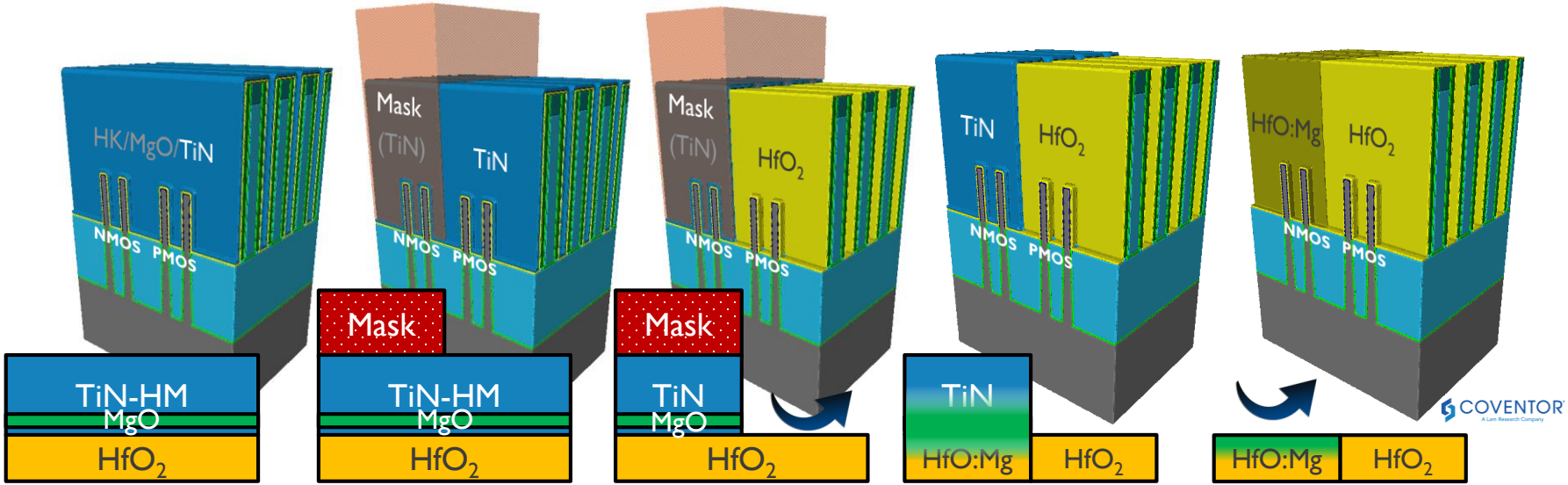
DIFFUSION AND GATE REPLACEMENT (D&GR) FLOW

VOLUME-LESS EWF TUNING

- D&GR* flow with n-type WF shifter e.g. MgO, LaO, ...

* R. Ritzenthaler (imec), IEDM 2014



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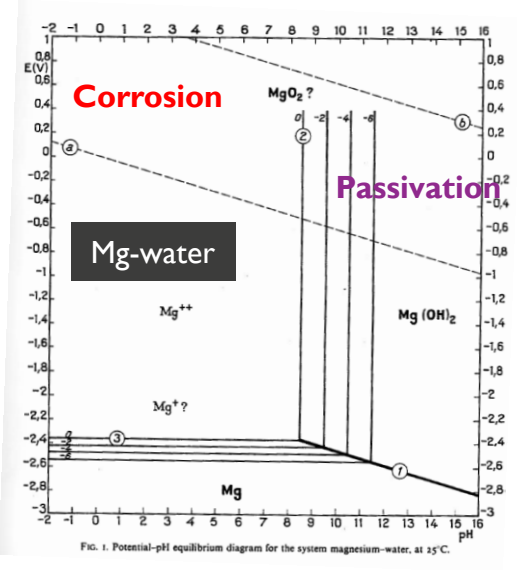
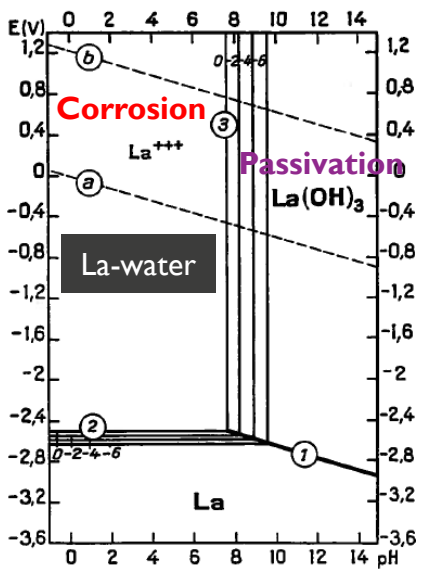
D&GR RISK ASSESSMENT – 1/2

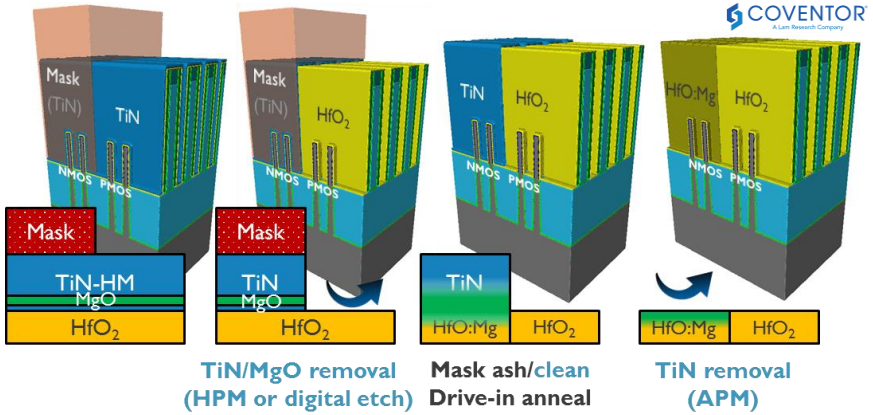
CORROSION

- Corrosive and hygroscopic MgO, LaO
  - Well optimized wet etching and rinsing solutions needed



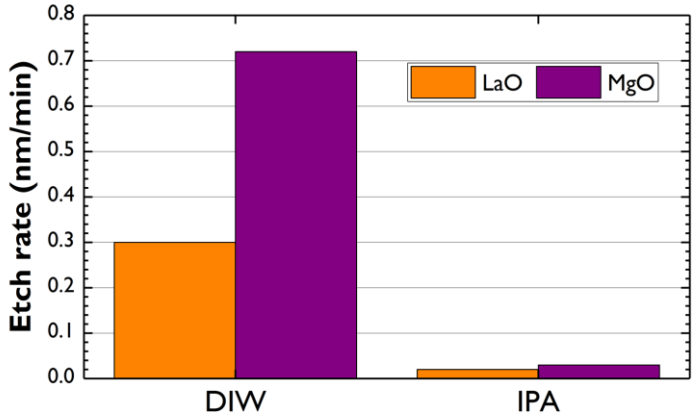


M. Pourbaix: "Atlas of Electrochemical Equilibria in Aqueous Solutions" (1974)
Mg-water: pp. 141, La-water: pp. 193.



TiN/MgO removal (HPM or digital etch)

Mask ash/clean
Drive-in anneal



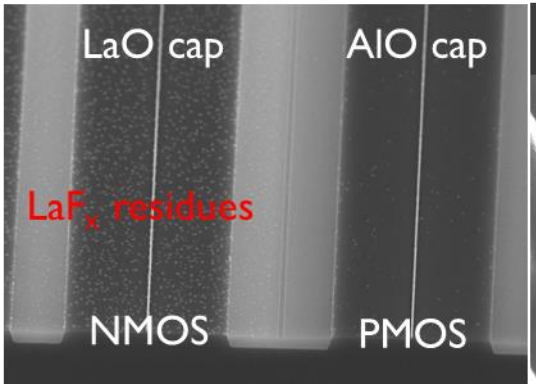
D&GR RISK ASSESSMENT – 2/2

NON-SOLUBLE FLUORIDE RESIDUES

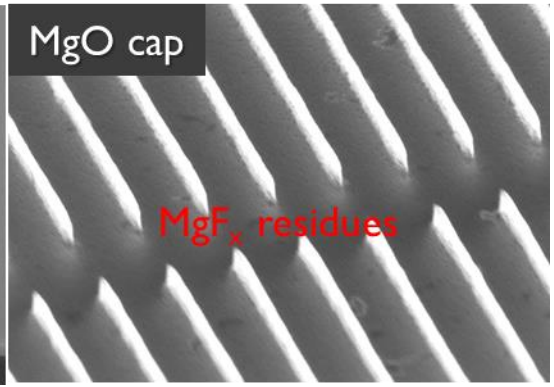
- Non-soluble fluoride residues to be generated if HfO:Mg, La exposed to fluorine containing chemistry (dry/wet)
  - LaFx, MgFx difficult to remove
  - Dry etch & post etch wet clean → fluorine free chemistries preferred

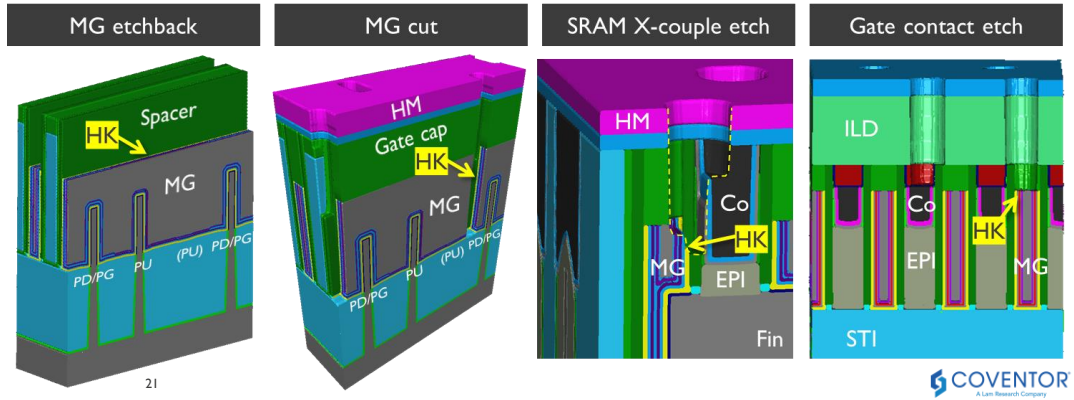
- Challenge/concern on PERR:
  - MGEB, MGC, x-couple, gate contact etches

Gate 1st planar:
Gate etch + HK removal (HF/HCl)



Gate 1st FinFET:
D&GR gate removal (HF + APM)





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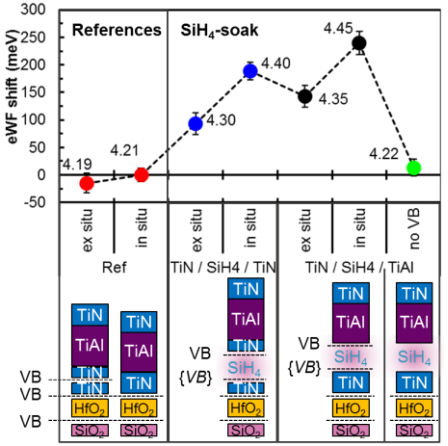
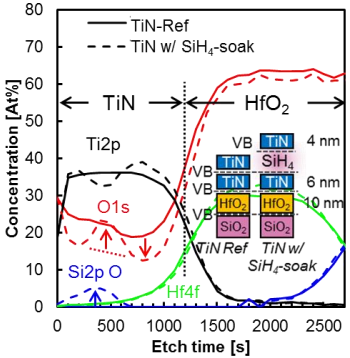
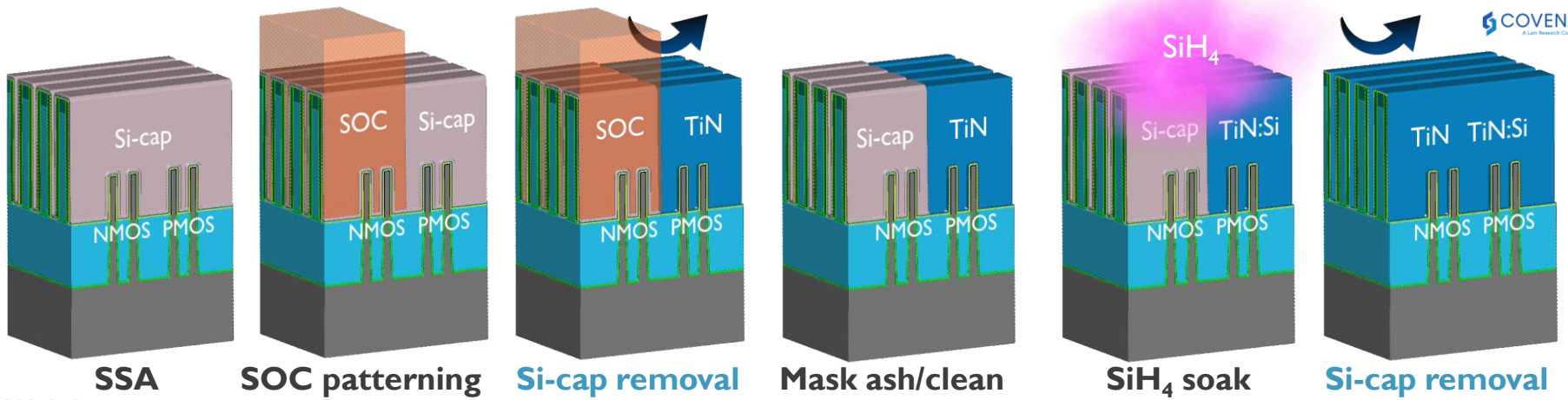
SiH_4 SOAK
ZERO-THICKNESS EWF TUNING

- SiH_4 soak: O scavenging from the TiN/HfO_2 interface
  - provides p-type Vt shift
  - zero-thickness eWF tuning
- NP patterning done by a thin liner HM + SiH_4 soak
  - e.g. SiH_4 soak after SSA (sacrificial Si-cap anneal):



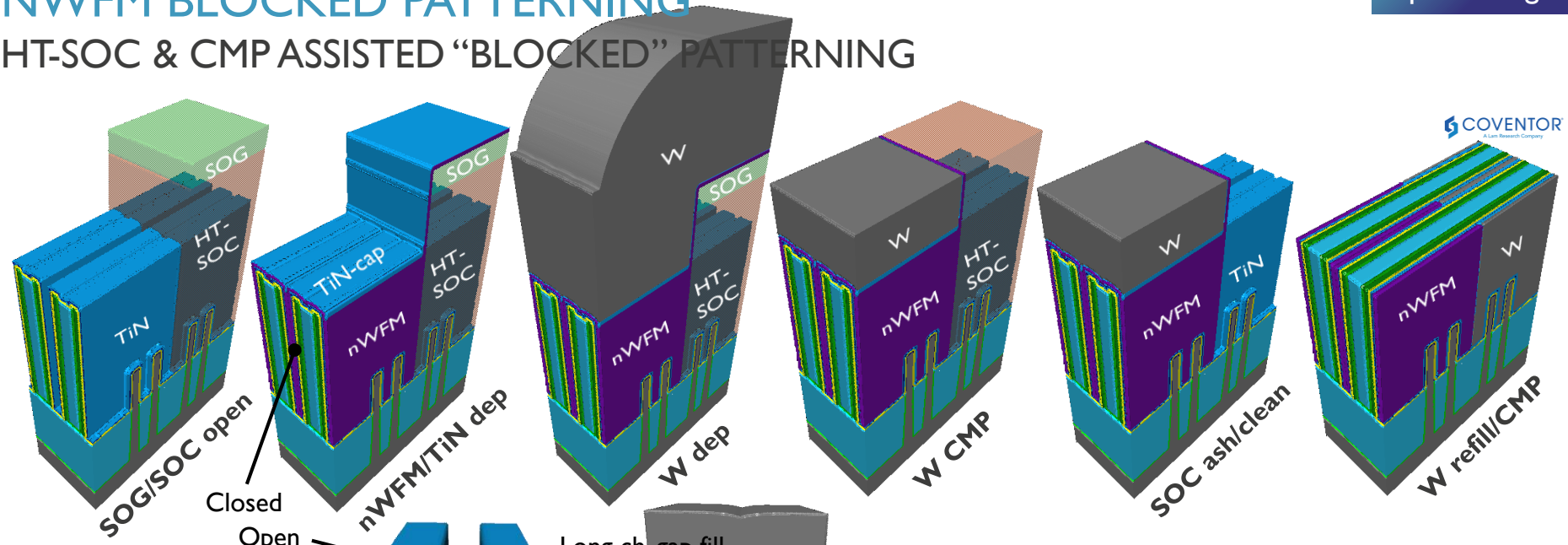


L-Å Ragnarsson (imec), VLSI 2016



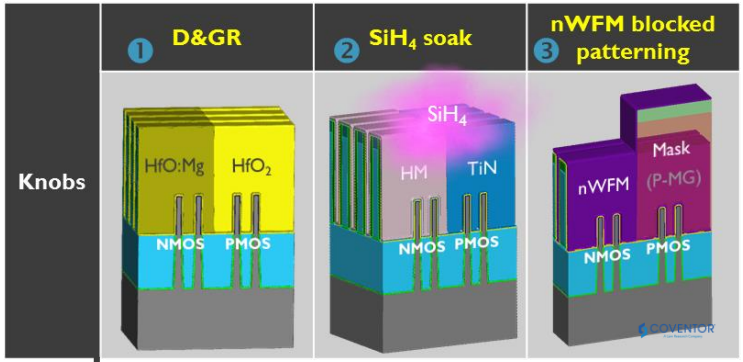
NWFM BLOCKED PATTERNING

HT-SOC & CMP ASSISTED "BLOCKED" PATTERNING



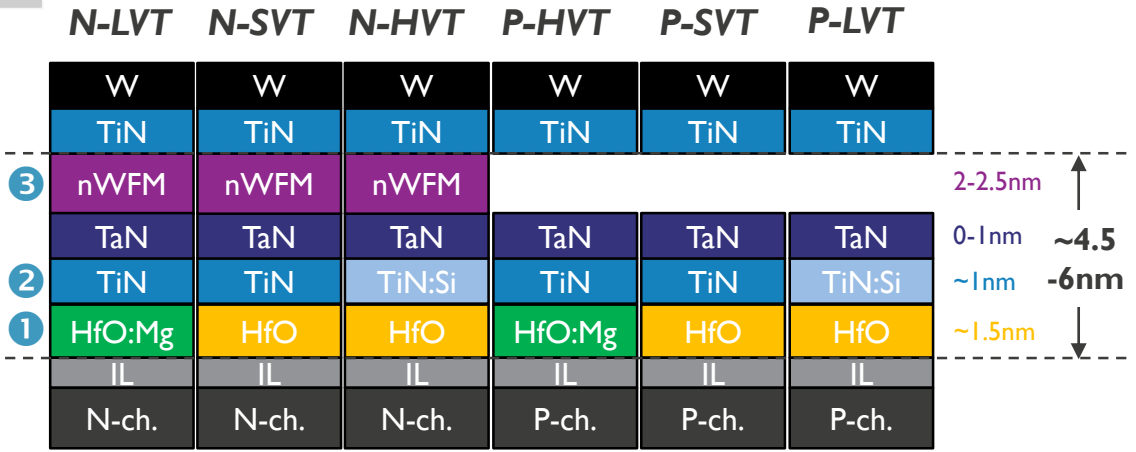
- CMP assisted "blocked" patterning
  - Enables closed gate patterning
  - Need thermally stable mask e.g. HT-SOC
  - No need for a wet metal etch!

ULTIMATE RMG SCALING
TOWARDS N5 AND BEYOND



- Dummy poly removal
- Core/IO oxide patterning
- HK deposition
- D&GR ❶
- HK cap dep
- SSA/Masked SiH_4 soak ❷
- Barrier dep (can skip)
- nWFM blocked patterning ❸
- W CMP

- Ultimate RMG scaling and multi-Vt enabled by combining several patterning knobs
  - e.g. D&GR + SiH_4 soak + blocked patterning



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SUMMARY

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RMG WET PROCESS CHALLENGES AND THE PATTERNING KNOBS

- RMG challenge
  - Not much space!
- RMG patterning development
  - Implementing tri-layer patterning (PR/SOG/SOC)
  - Digital wet etching of TiN successfully demonstrated
- RMG scaling & multi-V_t patterning knobs
  - ❶ **D&GR** to enable zero-thickness eWF tuning
  - ❷ **SiH_4 soak** as volumeless eWF tuning
  - ❸ **Blocked patterning** to pattern closed nWFM
  - Ultimate RMG scaling and multi-Vt patterning to be enabled by ❶+❷+❸

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