SELECTIVE ETCH REQUIREMENTS FOR THE NEXT GENERATION OF SEMICONDUCTOR DEVICES

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ON BEHALF OF THE SURFACE AND INTERFACE PREPARATION GROUP OF THE UNIT PROCESS DEPARTMENT
10TH OF APRIL 2018
I/O BANDWIDTH

POWER
- 500 Watt (mains level)
- 100 Watt
- 1 Watt (battery level)
- 100mWatt (battery level)
- 100µW (ambient level)

DATA STORAGE

IOT personal/home gateway
- High-performance mobile (low power)
- High performance CPU/GPU
- Mass Storage
- Hi-speed communication (Optical IO)

DATA CENTER/ CLOUD

IOT sensor nodes
- Ultra-low-power, cost-sensitive design
- Sensor and sensor integration

IOT interfaces

PERFORMANCE

- 1 Mbp/s
- 10 Mbp/s
- 1 Gbp/s
- 100 Gbp/s
- 1 Tbp/s

- 10 Mop/s
- 10 Gop/s
- 100 Gop/s
- 1 Top/s
- 1 Pop/s

1 TByte
1 TByte
100 GByte
10 GByte
100 MByte

IOT personal/home gateway

Data center/cloud

IOT sensor nodes

IOT interfaces

Ultra-low-power, cost-sensitive design
Sensor and sensor integration
DIMENSIONAL SCALING CHALLENGES, DEVICE ARCHITECTURE & MATERIAL INNOVATION

Happy scaling era
- # transistors per area doubles every two years for same cost
- Lithography driven scaling

90nm: BEOL
- Introduction of Cu (DD)

Less happy scaling era
- Still doubles but device scaling provides diminishing returns
- Material driven scaling

20 nm: First sign of trouble
- Double patterning (cost)
- Planar device runs out of steam

14nm: FinFET
- New architectures: FinFET device saves the day

10-7nm: More trouble
- Multi-patterning cost escalates
- Introduce Co in MOL

7-5nm: At last ...
- EUV reduces cost
- Towards ultimate fin scaling
- Introduction SiGe p-channel

3-2.5nm: GAA
- Fin based device runs out of steam?
- Horizontal or Vertical nanowire, hybrid materials

Highly scaled new device architectures
- CFET, VFET, 2D, spin, ...

3Fin → 2Fin → 1Fin?

Scaling boosters
- RMC, SAGC, MG cut, FAV, BPR, SAB, ...

3D FinFET
- 22nm pitch
- 120nm STI

Ultimate finFET
- 170nm STI

Introduction
- SiGe p-channel

2.5nm

Material driven scaling
- Scaled new device architectures
- CNT FET


year
DIMENSIONAL SCALING CHALLENGES, DEVICE ARCHITECTURE & MATERIAL INNOVATION

DIMENSIONAL SCALING: LITHOGRAPHY DRIVEN

Happy scaling era
# transistors per area doubles every two year for same cost
Lithography driven scaling

Happy scaling era
# transistors per area doubles every two year for same cost
Lithography driven scaling

Last ...
Cost...

Fin based device runs out of steam?
Horizontal or Vertical nanowire, hybrid materials

90nm: BEOL
Introduction of Cu (DD)

90nm: BEOL
Introduction of Cu (DD)

3-2.5nm: GAA
Fin based device runs out of steam?
Horizontal or Vertical nanowire, hybrid materials

2011
2013
2015
2017
2019
2021
2023
2025
2027

8 Fin

Planar: HKMG

28nm
20nm
2009
2007
2005

14nm
22nm pitch
22nm pitch

20nm: First sign of trouble
Double patterning (cost!)
Planar device runs out of steam

10nm
7nm
2.5nm
3nm

5nm: More trouble
Multi-patterning cost escalates
Introduce Co in MOL

Planar: Strained Si

Planar: HKMG

90nm: BEOL
Introduction of Cu (DD)
DIMENSIONAL SCALING CHALLENGES, DEVICE ARCHITECTURE & MATERIAL INNOVATION

DIMENSIONAL SCALING: LITHOGRAPHY DRIVEN

AREA SCALING: PITCH SCALING AND SCALING BOOSTERS
PROCESS INNOVATION REQUIRED ON TOP OF GEOMETRICAL SCALING

Happy scaling era
# transistors per area doubles every two years for same cost
Lithography driven scaling

Less happy scaling era
Still doubles but device scaling provides diminishing returns
Material driven scaling

1933 PATTERNING
DRAM
LOGIC
2DNA

14nm
20nm
28nm
40nm
90nm
65nm
90nm
14nm
20nm
28nm
40nm

Highly scaled new device architectures

3-2.5nm: GAA
Fin based device runs out of steam?
Horizontal or Vertical nanowire, hybrid materials

CFET, VFET, 2D, spin, ...

AV, BPR, SAB, ...

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SiGe p-channel

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DIMENSIONAL SCALING: LITHOGRAPHY DRIVEN

AREA SCALING: PITCH SCALING AND SCALING BOOSTERS

PROCESS INNOVATION:

DEVICE ARCHITECTURE IMPACTS ELECTROSTATICS

3-2.5nm: GAA
Fin based device runs out of steam?
Horizontal or Vertical nanowire, hybrid materials

Highly scaled new device architectures

CFET, VFET

Stanford IEDM'14

CNT FET

28-32nm
Bulk Planar
(V_{dd} ~ 0.9-1.0V)
DIMENSIONAL SCALING CHALLENGES, DEVICE ARCHITECTURE & MATERIAL INNOVATION

DIMENSIONAL SCALING: LITHOGRAPHY DRIVEN

AREA SCALING: PITCH SCALING AND SCALING BOOSTERS

PROCESS INNOVATION PATH

DEVICE ARCHITECTURE IMPACTS ELECTROSTATICS

IMEC HIGH PERFORMANCE MOBILE LOGIC ROADMAP

3-2.5nm: GAA
Fin based device runs out of steam?
Horizontal or Vertical nanowire, hybrid materials

Happy scaling era
# transistors per area doubles every two year for same cost
Lithography driven scaling
AS SCALING CONTINUES, CHALLENGES ARISE IN WET PROCESSING

Wetting and kinetics for nanostructured surfaces

- Capillary force induced pattern collapse
- Selective etch requirements

3D structures with more surface area → interfacial phenomena

- Actual wetting states confirmed by optical reflectometry; Xu et al., ACS Nano (2014).

- Low k: 45 nm L/S, AR~5
- Si pillars AR~20
- Si fins AR~10

- in-situ TEM observations
- Xu et al., Mirsaidov, Semicon Korea (2017).

- High surface to volume ratio → mechanical stability and structural integrity

- Dimensional scaling → introduction of new device architectures and new selective etch requirements

- Cu recess to enable FSAV

- STI oxide recess, SiNx compatible

- Si NW release VLSI 2016
- Si NS release IFT 2017
<table>
<thead>
<tr>
<th>Wetting</th>
<th>electrical double layers</th>
<th>water structuring</th>
</tr>
</thead>
<tbody>
<tr>
<td>Differentiation between Wenzel / Cassie-Baxter / Mixed wetting states</td>
<td>Overlap of electrical double layers (EDL) in nanochannel</td>
<td>Water confinement</td>
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<tr>
<td>In-situ study of wetting stability and hysteresis on initially non-wetting substrate</td>
<td>Depletion of ions with same charge as surface in channel: no electroneutrality</td>
<td>Formation of ice-like water in nanoconfined volumes</td>
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</table>

- Wetting hysteresis observed (Vrancken et al., Langmuir 2017).
- pH shift expected (D.Bottenus et al., Lab on Chip, 2009, 9, 219.)
- Depletion etchants (A. Okuyama et al., Solid State Phenom. 2015, 219, 115.)
- Effect of water structuring on diffusivity of chemical species in nano-confined volumes expected

(a) IPA concentration profile oscillating around the critical concentration and (b) the corresponding wetted area fraction as a function of time.
CAPILLARY FORCE INDUCED PATTERN COLLAPSE
IN SITU CHARACTERIZATION OF DEWETTING AT NANOSCALE

- Real-time visualization of pattern collapse with TEM in liquid cell.
- Polycrystalline Si nanopillars, height ≈ 450 nm.
- Formation of clusters due to capillary instabilities.

- During drying the water film becomes unstable, and water is drained gradually towards bended nanopillars islands.
PATTERN COLLAPSE/STICITION FREE DRYING

- Replace water by low surface tension ($\gamma$) solvents to reduce capillary force;
- Improve evaporation rate (gas flow and heat);
- Improve on IPA quality.

Si nanopillars with native oxide:

<table>
<thead>
<tr>
<th>Solvent</th>
<th>$\gamma$ (N/m)</th>
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<tbody>
<tr>
<td>DIW</td>
<td>0.072</td>
</tr>
<tr>
<td>IPA</td>
<td>0.022</td>
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Increase surface hydrophobicity reduces pattern collapse in water (not necessarily for other solvents!)

Reduce capillary force by increasing contact angles ($\theta$) of rinsing liquids;
Reduce surface adhesion force, more relevant when IPA dry is used after SFC;
Further reduction capillary force: towards sublimation drying.

Surface functionalizing chemistry (SFC)
SELECTIVE ETCH REQUIREMENTS
SEMICONDUCTOR ETCH: GAA SELECTIVE ETCH REQUIREMENTS

Wostyn et al., ECS (2015).
Witters, VLSI2017.
Mertens et al., IEDM (2017).
SEMICONDUCTOR ETCH: GAA SELECTIVE ETCH REQUIREMENTS

Anisotropic selective etch. Process time ~ hour

Isotropic selective etch. Process time ~ min

For both HCl (g) and formulated mixture, selectivity increases strongly with increasing Ge%.

DIELECTRIC ETCH

FinFET/GAA/CFET/VFET

Si/SiGe, GAA Fin reveal (SiO$_2$/SiN etch)

GAA inner spacer EB [SiN(OC) etch]

CESL removal (SiN etch)

Oxide recess selective to SiNx

Isolation recess (SiO$_2$/SiN etch)

Bottom isolation recess (SiO$_2$ etch)

N/P isolation recess (SiO$_2$/SiN etch)

BPR isolation recess

Selective SiNx removal for 3D-NAND fabrication

3D SCM dummy gate recess

Mertens et al., IEDM (2017).
Pacco et al., SPCC (2018)
DIELECTRIC ETCH

SiGe/Si fin protection by SiN STI liner

Prevention of SiGe oxidation and Ge diffusion by SiN STI liner demonstrated

SiN recess

Mertens et al., IEDM (2017).
Pacco et al., SPCC (2018)
**METAL ETCH**

**Selective removal**

- **IC: MHM/ESL removal**
  - TiN-HM (and TiFx residue) removal

- **RMG WFM patterning**
  - WFM removal in limited spaces

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**Controlled metal recess: BPR, FSAV, SAGC, CMR**

- **BPR metal recess**
- **Fully Self Aligned Via**

**Vertical GAA-NWFETs**

- Oniki et al., SPCC (2018).
CORE CMOS PARTNERS

LOGIC / MEMORY IDM & FOUNDRIES

FABLESS & FABLITE

EQUIPMENT & MATERIAL SUPPLIERS / OSAT / EDA / JDP PARTNERS
embracing a better life