Chemical/Mechanical Balance Management through Pad Microstructure in Si CMP

Post CMP Cleaning Austin 2017 | Ratanak Yim (Viorel Balan)

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Perfect surface quality in order to build the 2\textsuperscript{nd} transistor

Planarization Challenges:
- Si Thickness Control: SPEC < 10nm + Si Range < 1nm

Excellent Silicon Surface Quality with Low Material Consumption
Outline

- Chemical and Mechanical Synergy of the CMP Process
  - Chemical action
  - Mechanical action

- Correlation Results Between Wafer Surface Quality and Pad Microstructure in Advanced Si CMP

- Conclusion
CMP: CoMPlex Process

**SYNERGY** between:

- **CHEMICAL action**: SLURRY Chemistry
- **MECHANICAL action**: PAD + Abrasive particles

**Surface Chemical Modification**

**Mechanical Removal**

**Material**

Chemical/Mechanical Balance to Adapt to Each CMP Process
Pad Characteristics and its Actions

The Pad Plays a Major Role in the Chemical/Mechanical Balance of the CMP Process

**CHEMICAL action**
- **Pores** + Grooves
  - Slurry Transport

**MECHANICAL action**
- **Pores** + Asperities
  - Wafer Contact

Polishing
## Pad Porosity

<table>
<thead>
<tr>
<th>Item</th>
<th>Pore size</th>
<th>Porosity</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pad A</td>
<td>Extra Small</td>
<td>Medium</td>
</tr>
<tr>
<td>Pad B</td>
<td>Small</td>
<td>High</td>
</tr>
<tr>
<td>Pad C</td>
<td>Small</td>
<td>Extreme high</td>
</tr>
<tr>
<td>Pad D</td>
<td>Large</td>
<td>High</td>
</tr>
</tbody>
</table>

Advanced Polishing Pad

Conventional Polishing Pad

**SEM Cross section**

4 Pads with Different Pore Sizes and Porosities Evaluated for Advanced Si CMP
Blanket Silicon Wafer Polishing Conditions

**Consumables:**
- Pad: Dow Pads
- DD: 3M Brush or AF38 DD
- Slurry: High Purity Colloidal Silica

**Process Conditions:**
- Pressure: 1.5psi
- Rotation: Platen at 43 rpm
- Flow: 200 ml/min
- Downforce: 7 lbf (ex-situ conditioning)

**Polishing Tool:** LK PRIME™

- Only one CMP process step

**Same Conditioning to Compare Intrinsic Pad Properties**
Pad and Wafer Characterizations

Pad Characterization:
- Experimental
- 3D Topography
- Custom Data Analysis
- Pad Roughness Parameters
- Height Distributions
- Asperities Properties

Wafer Characterization:
- Si Wafer
- Wafer AFM Topography
- Wafer AFM Distribution
- Wafer Surface Roughness
- AFM Height Distributions
- Defect Level (SP2)
- Si RR (Precision Balance)

Wafer Surface Quality = f (Pad Texture Parameters)
Pad & Wafer Roughness Correlation Results

Low Pad Surface Roughness = Low Wafer Surface Roughness
Pad & Wafer Roughness Correlation Results

Low Pad Surface Roughness = Low Wafer Surface Roughness
Wafer Surface Quality Sq

Wafer Surface Quality

Lower Post CMP SI Roughness with Smaller Pad Asperities

Wafer Surface Roughness Driven by Pad Asperities Height: Atomic Si Planarization
Pad Texture Open

Texture Open = *Empty Volume/Projected Area*

Low Pore Size = Low Texture Open
Pad Texture Open Impact on RR & Sq

Increasing Open Pad Texture Increase RR but Decrease Surface Quality → Chemical Effect of Slurry
Increasing Open Pad Texture Increase RR and Decrease Defectivity Level
Si Wafer Quality Surface & Pad Texture Open

Chemical / Mechanical Balance in Si CMP Can Be Managed Through Pad Microstructure

Conventional Pad
Large Pore Size
= CHEMICAL action

Advanced Pad
Small Pore Size
= MECHANICAL action

Higher Si Removal Rate with High Texture Open
Conclusion

Chemical/Mechanical Balance Management through Pad Microstructure
Advanced Pad & Advanced Wafer Characterizations:
Better Understanding of Roughness Transfer from Pad to Wafer
Achieve Better CMP Performance
Thank you for your attention

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