



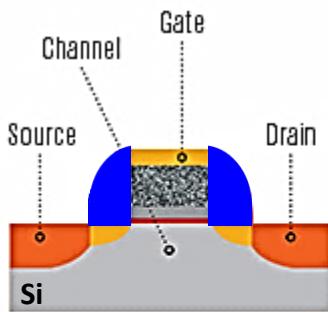
Chemical/Mechanical Balance Management through Pad Microstructure in Si CMP

Post CMP Cleaning Austin 2017 | Ratanak Yim (Viorel Balan)

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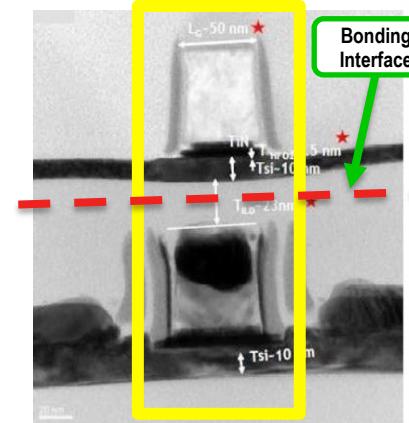
Si CMP Challenges for 3D Monolithic CoolCube™



1

First gate
fabrication

Si CMP



5

Planarization Challenges:

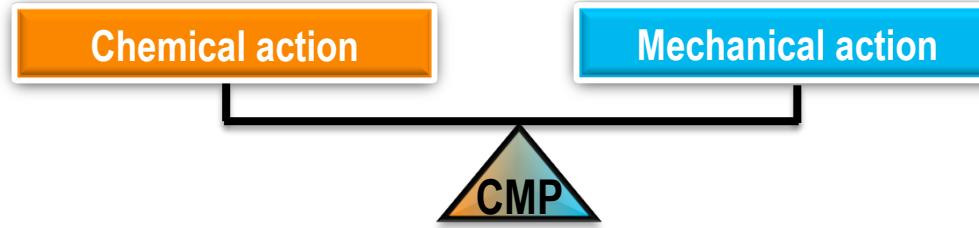
- Si Thickness Control :SPEC < 10nm + Si Range < 1nm

Perfect surface quality in order to build
the 2nd transistor

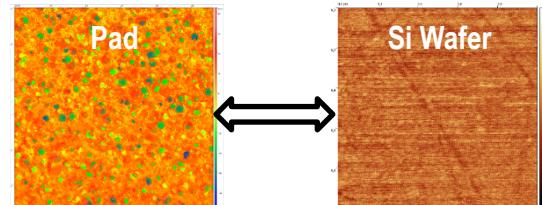
Excellent Silicon Surface Quality with Low Material Consumption

Outline

- Chemical and Mechanical Synergy of the CMP Process

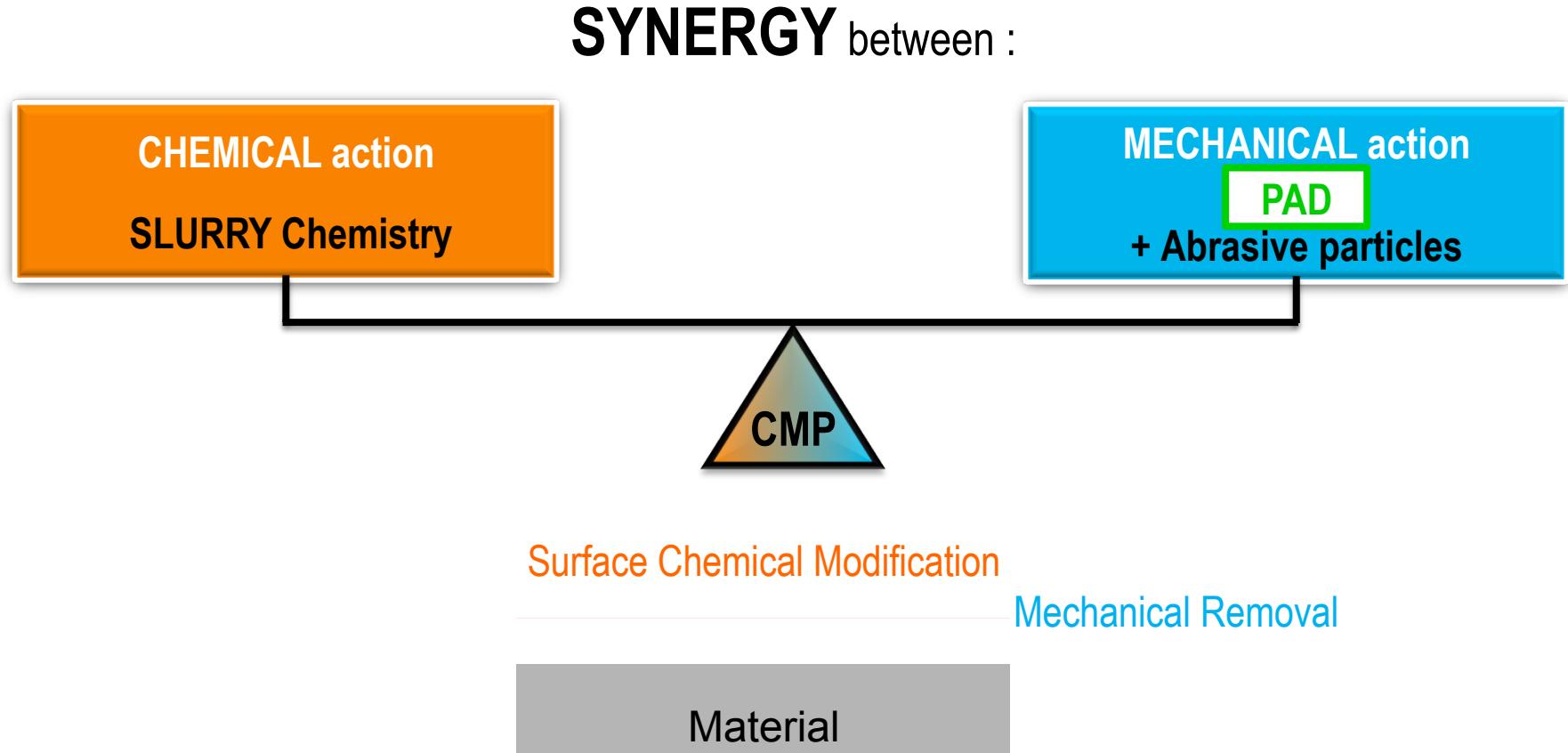


- Correlation Results Between Wafer Surface Quality and Pad Microstructure in Advanced Si CMP



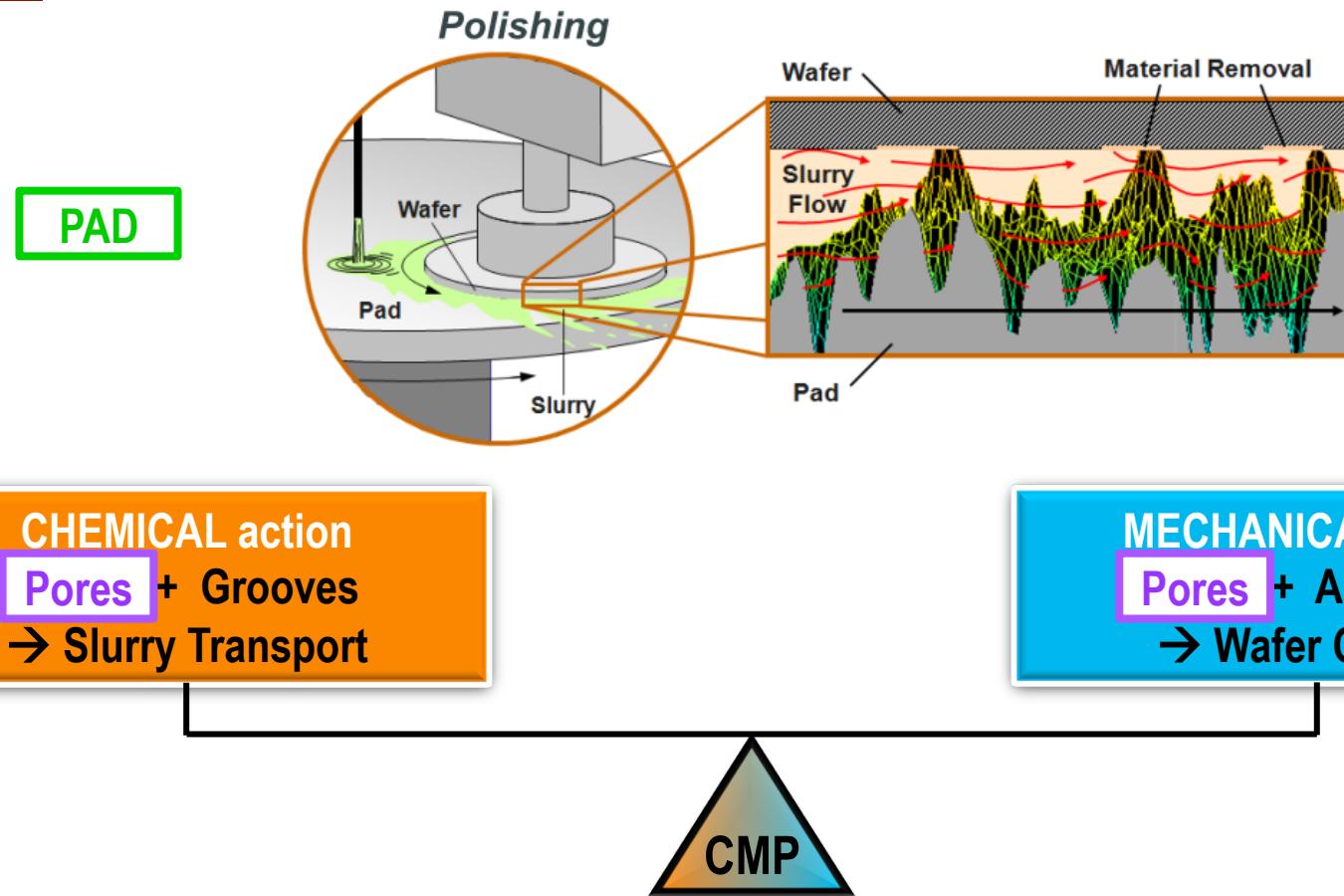
- Conclusion

CMP: CoMPlex Process



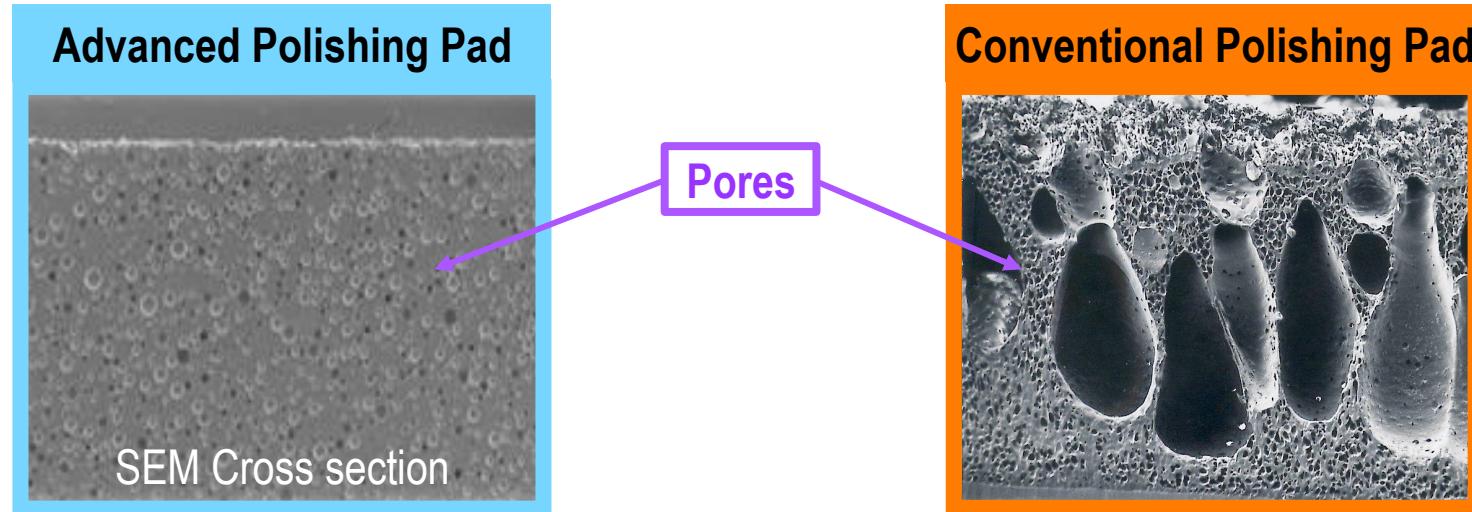
Chemical/Mechanical Balance to Adapt to Each CMP Process

Pad Characteristics and its Actions



The Pad Plays a Major Role in the Chemical/Mechanical Balance of the CMP Process

Pad Porosity

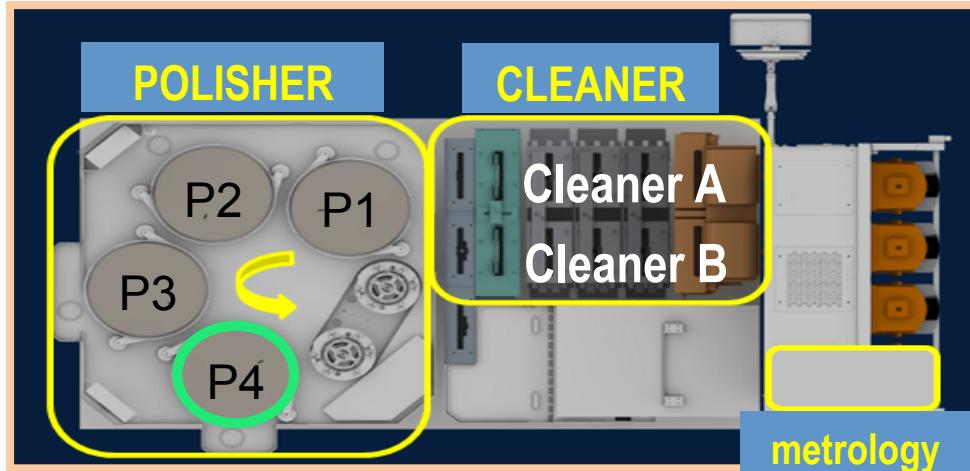


Item	Pore size	Porosity
Pad A	Extra Small	Medium
Pad B	Small	High
Pad C	Small	Extreme high
Pad D	Large	High

4 Pads with Different Pore Sizes and Porosities Evaluated for Advanced Si CMP

Blanket Silicon Wafer Polishing Conditions

Polishing Tool: LK PRIME™



- Only one CMP process step

Consumables:

- Pad: Dow Pads
- DD: 3M Brush or AF38 DD
- Slurry: High Purity Colloidal Silica

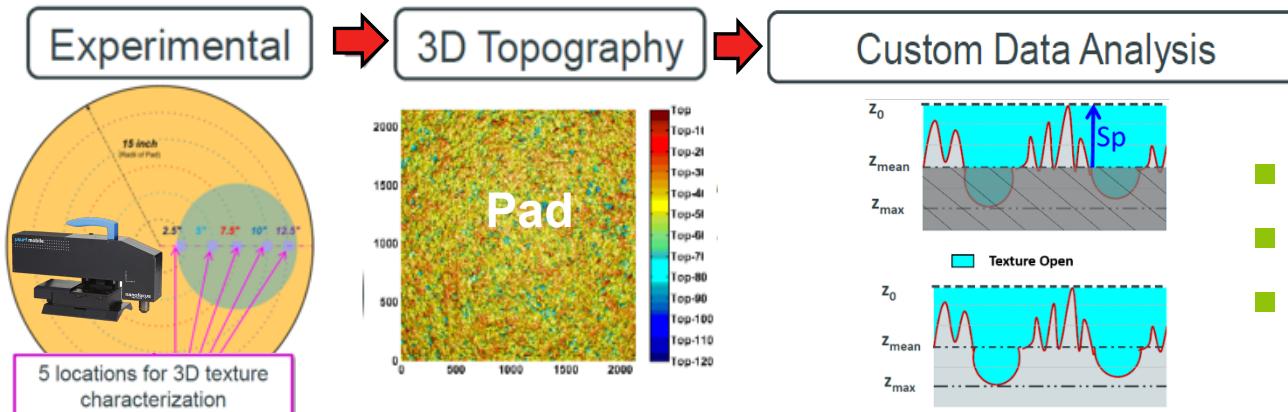
Process Conditions:

- Pressure: 1.5psi
- Rotation: Platen at 43 rpm
- Flow: 200 ml/min
- Downforce: 7 lbf (ex-situ conditioning)

Same Conditioning to Compare Intrinsic Pad Properties

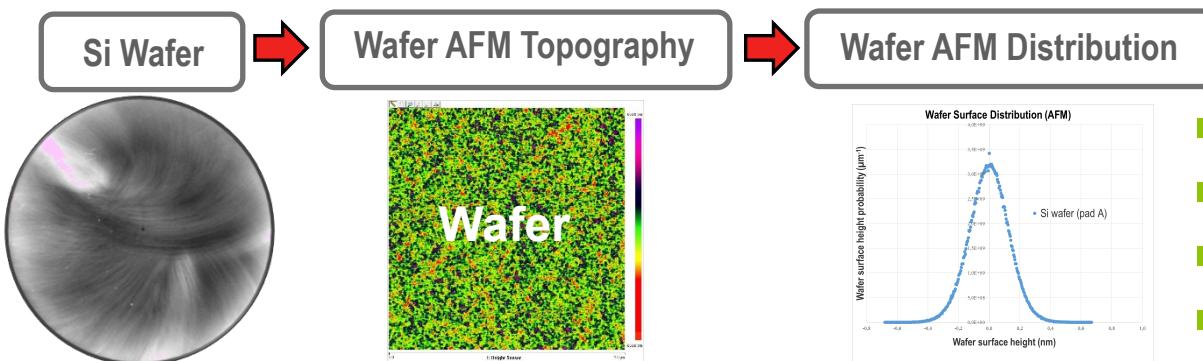
Pad and Wafer Characterizations

Pad Characterization:



- Pad Roughness Parameters
- Height Distributions
- Asperities Properties

Wafer Characterization:

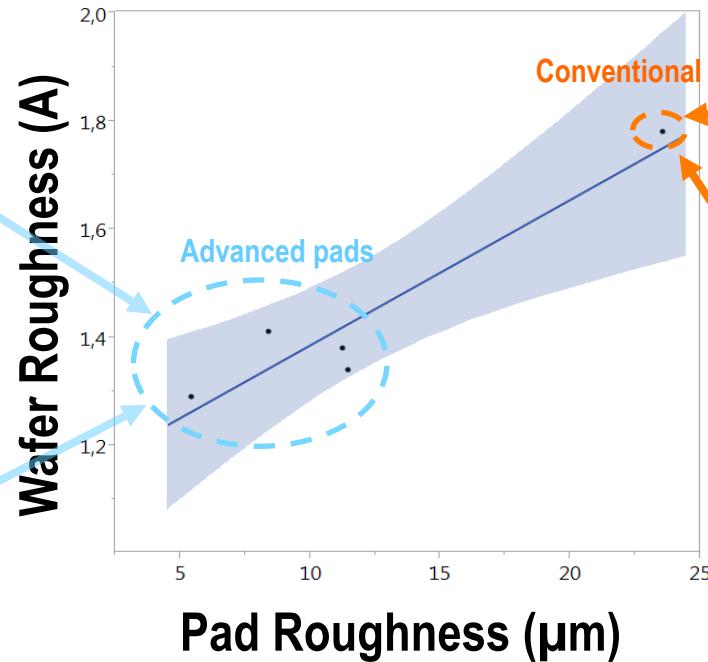
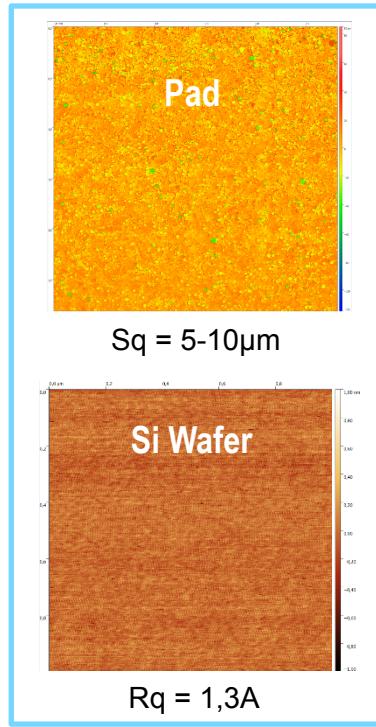


- Wafer Surface Roughness
- AFM Height Distributions
- Defect Level (SP2)
- Si RR (Precision Balance)

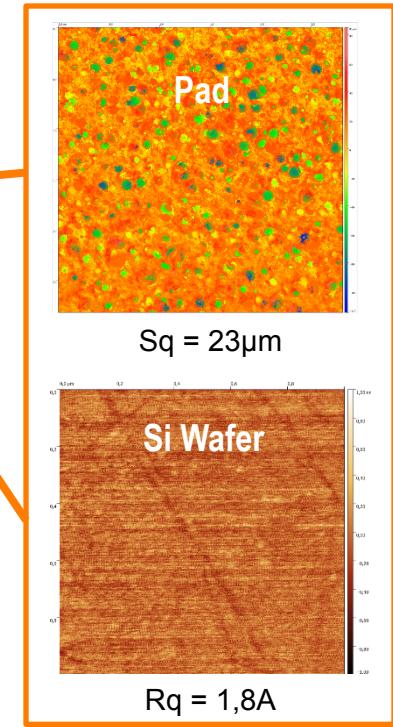
Wafer Surface Quality = f (Pad Texture Parameters)

Pad & Wafer Roughness Correlation Results

Advanced Polishing Pad



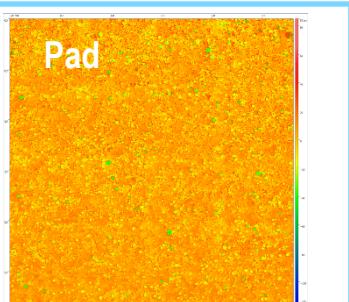
Conventional Polishing Pad



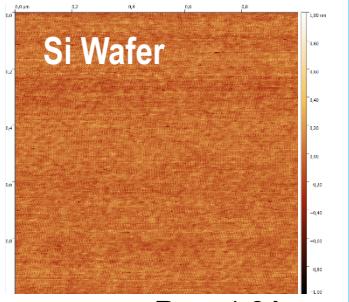
Low Pad Surface Roughness = Low Wafer Surface Roughness

Pad & Wafer Roughness Correlation Results

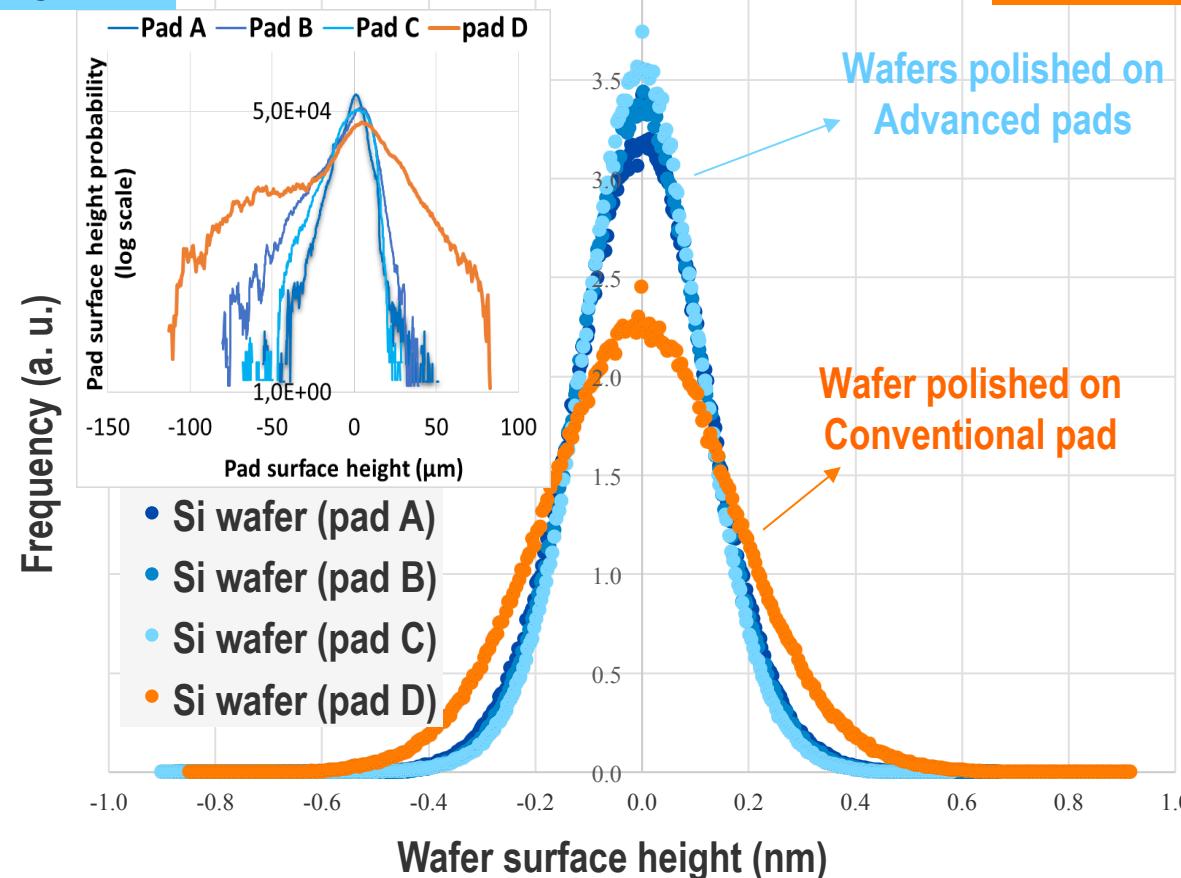
Advanced Polishing Pad



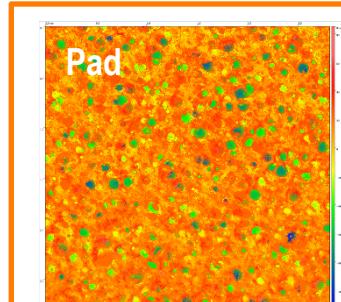
$S_q = 5\text{-}10\mu\text{m}$



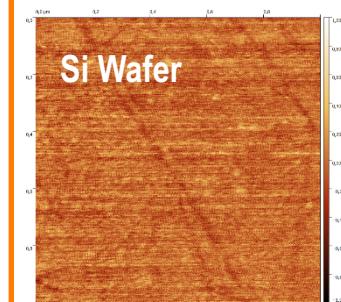
$R_q = 1.3\text{\AA}$



Conventional Polishing Pad



$S_q = 23\mu\text{m}$

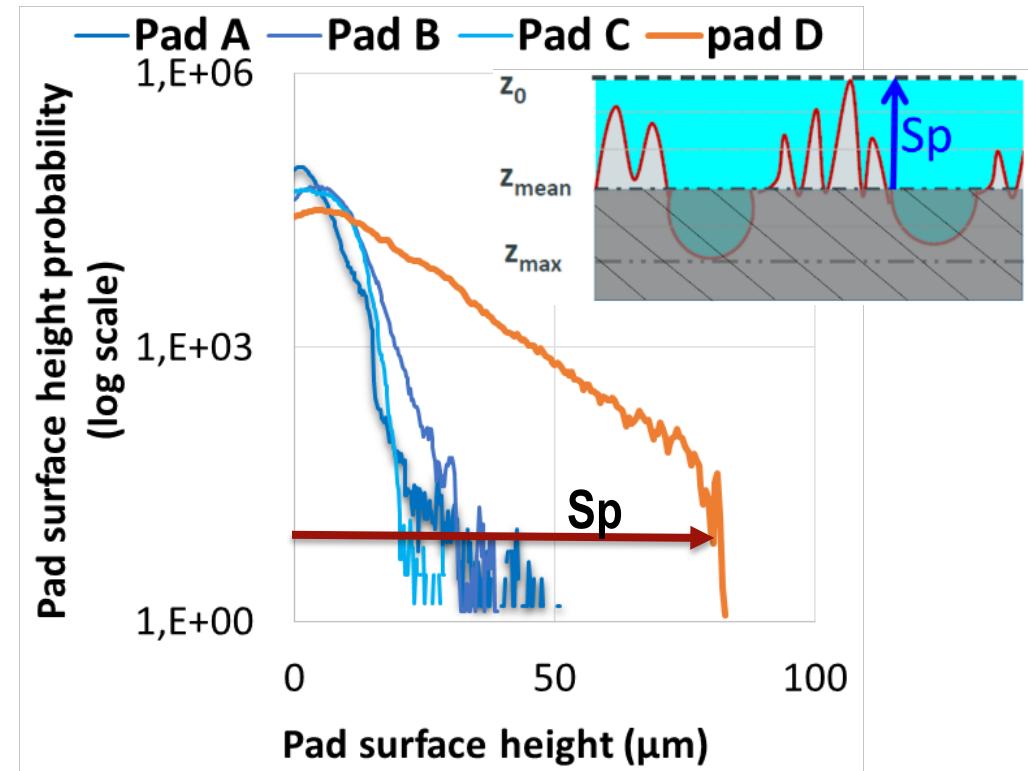
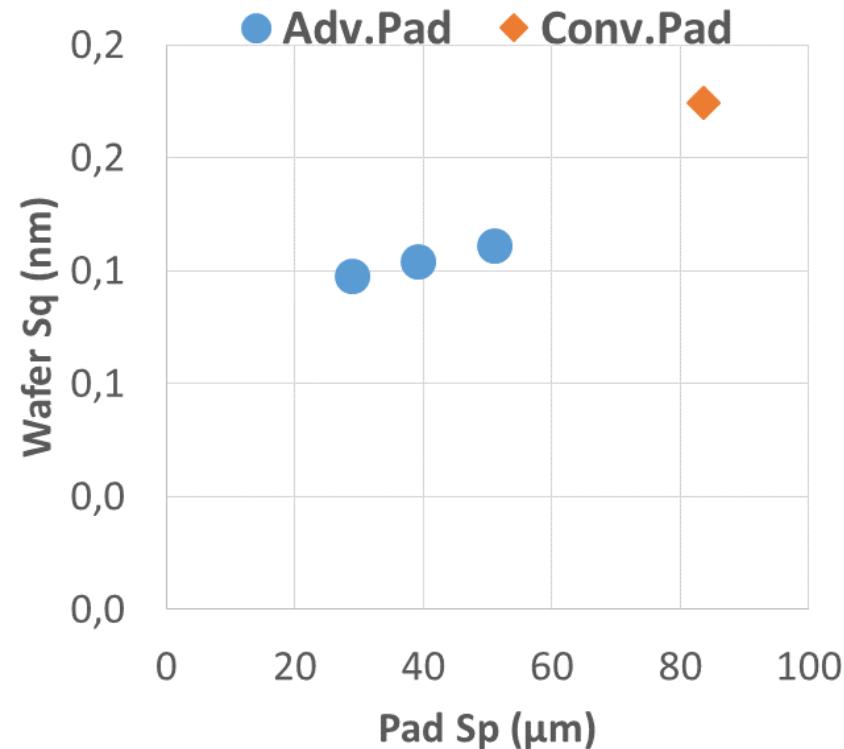


$R_q = 1.8\text{\AA}$

Low Pad Surface Roughness = Low Wafer Surface Roughness

Wafer Surface Quality Sq

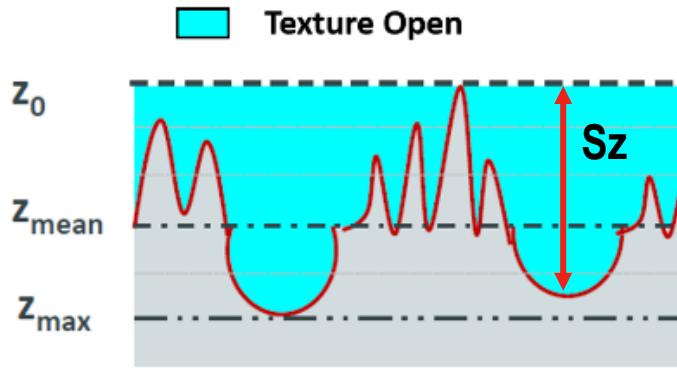
Wafer Surface Quality



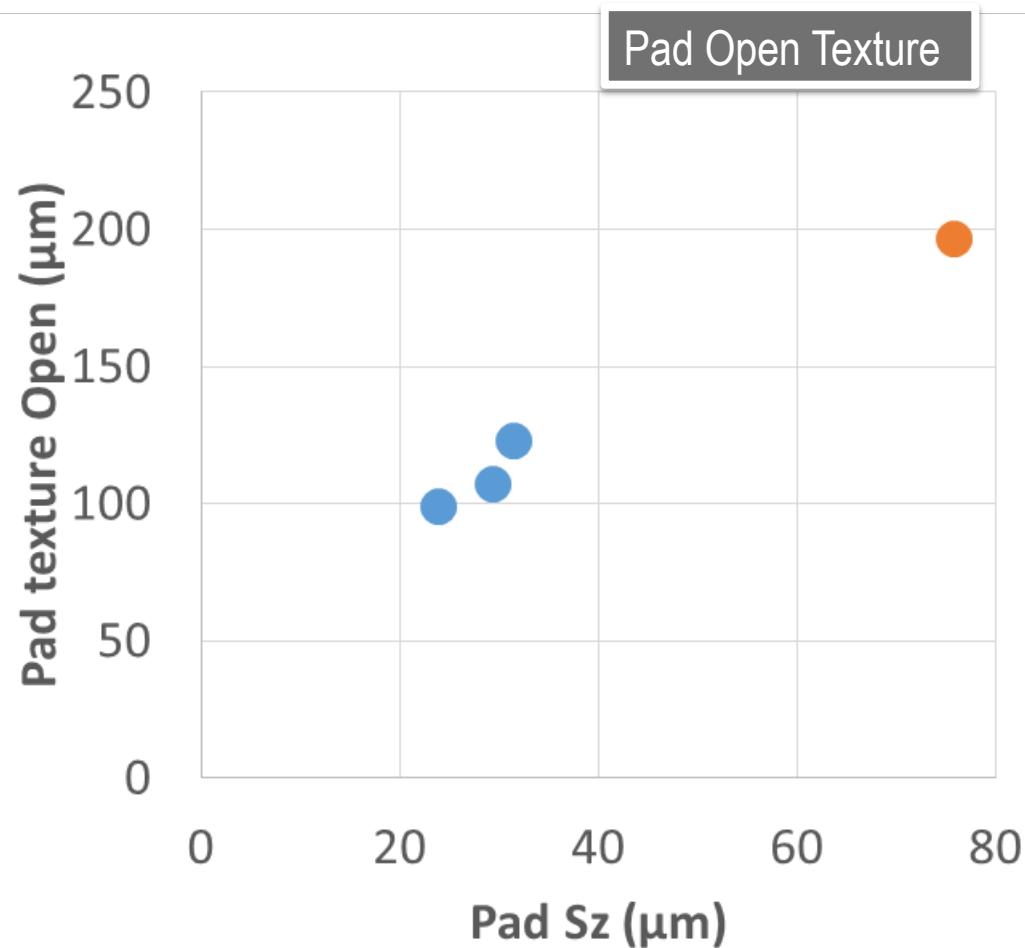
Lower Post CMP Si Roughness with Smaller Pad Asperities

Wafer Surface Roughness Driven by Pad Asperities Height: Atomic Si Planarization

Pad Texture Open



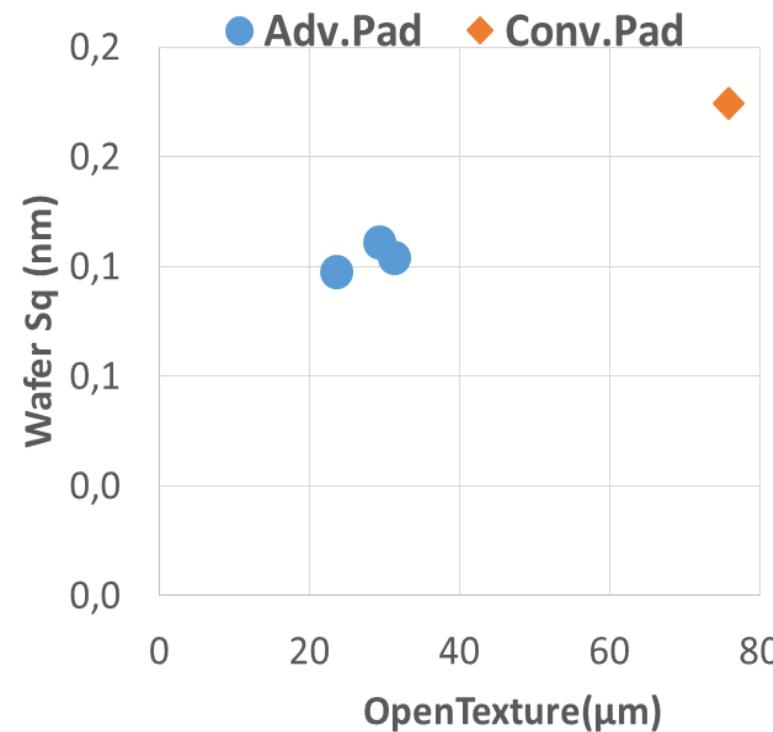
Texture Open = *Empty Volume/Projected Area*



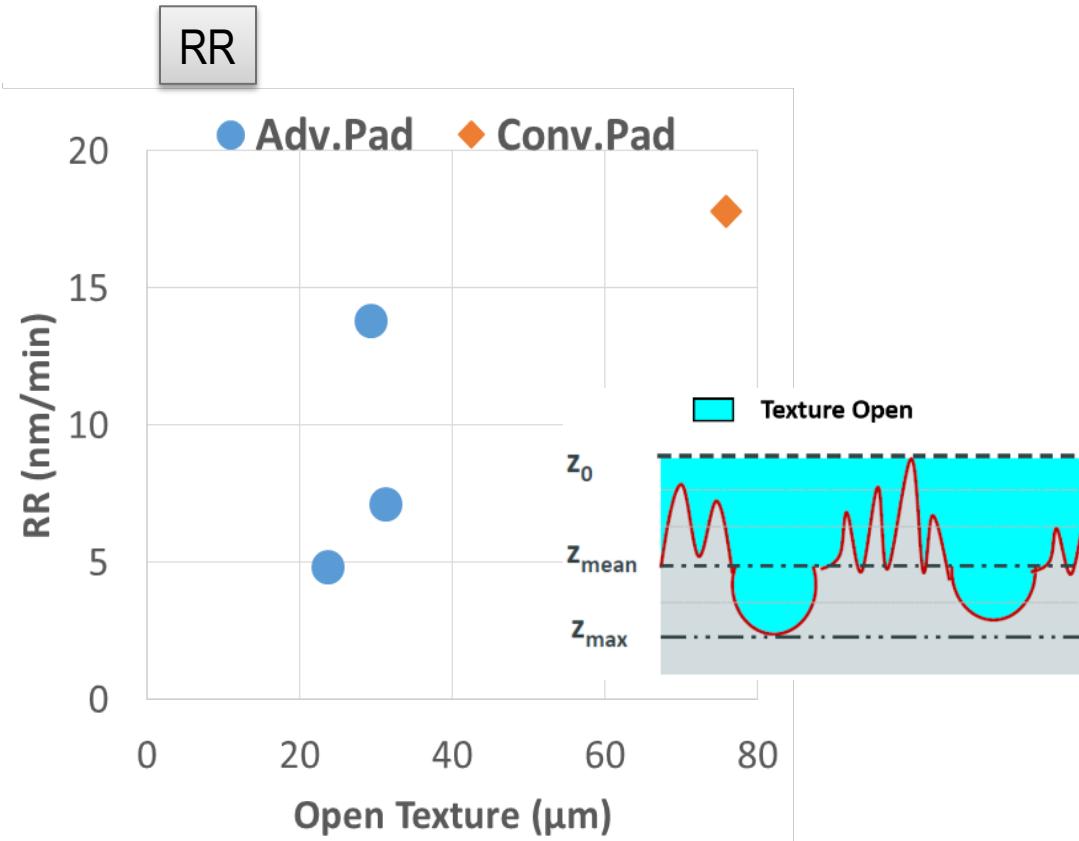
Low Pore Size = Low Texture Open

Pad Texture Open Impact on RR & Sq

Wafer Surface Quality



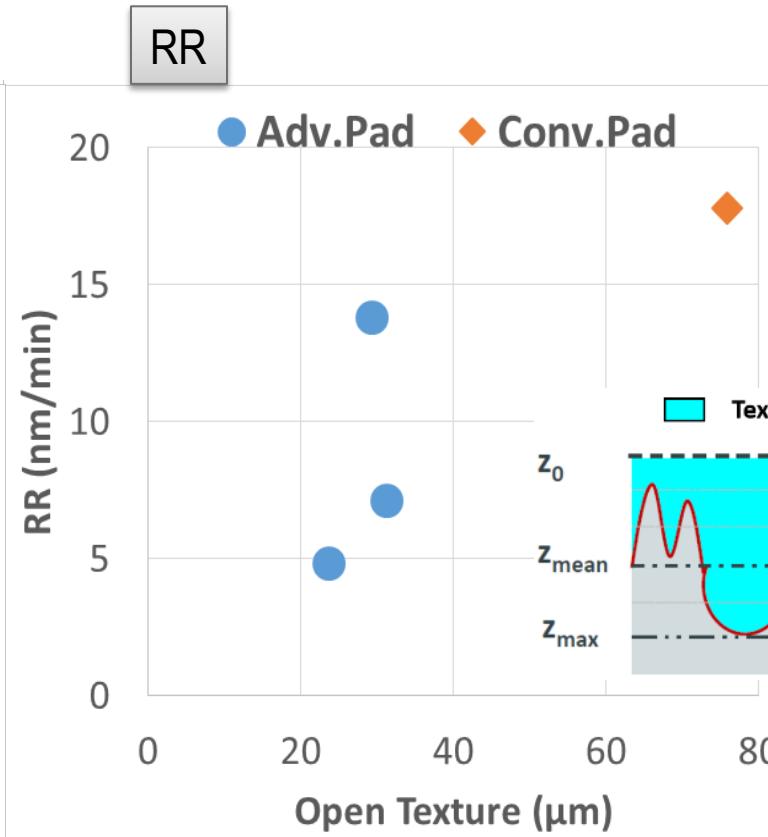
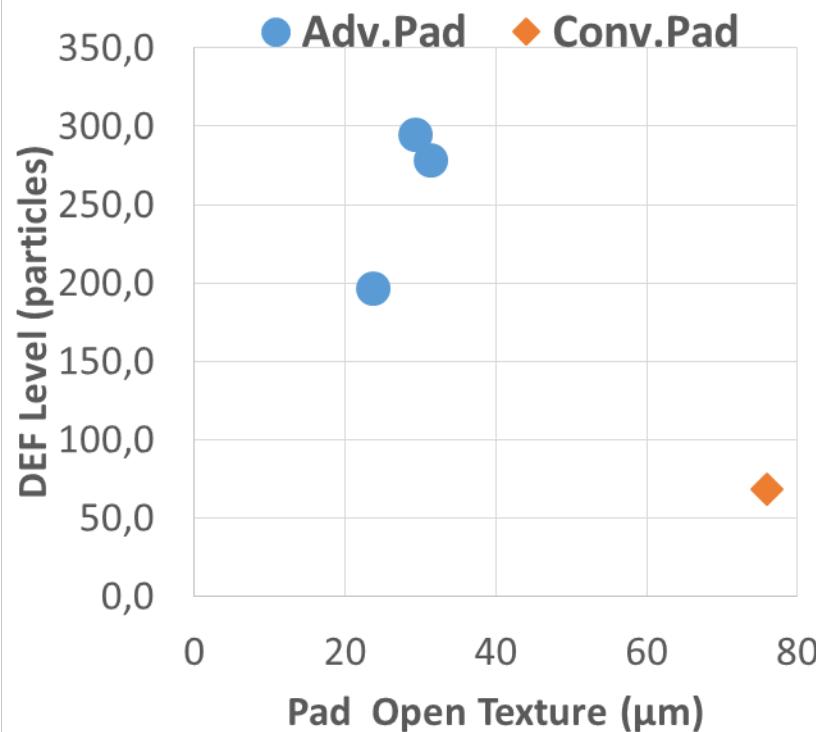
RR



Increasing Open Pad Texture Increase RR but Decrease Surface Quality →
Chemical Effect of Slurry

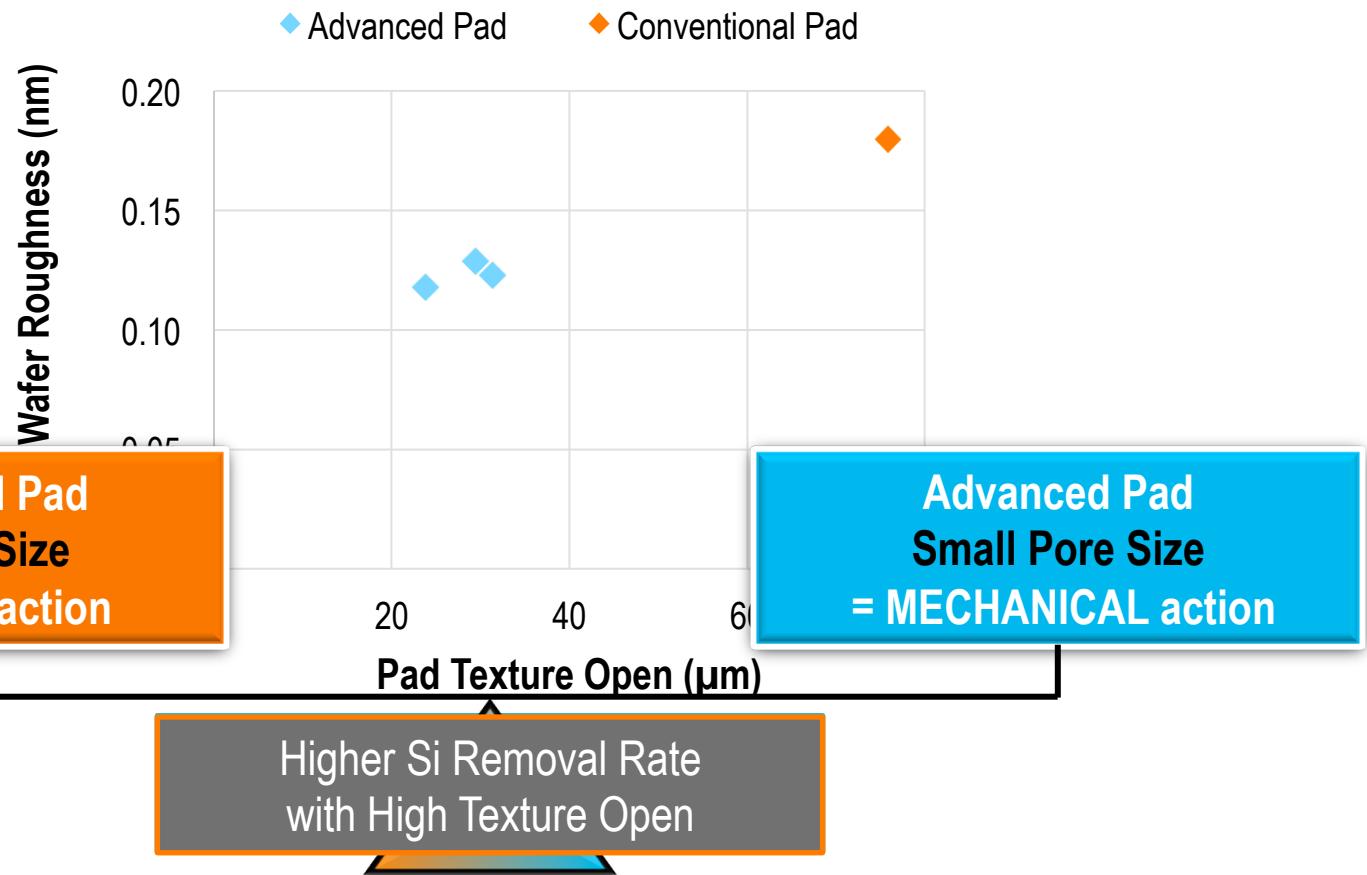
Pad Texture Open Impact on RR & Defectivity

Post CMP DEF



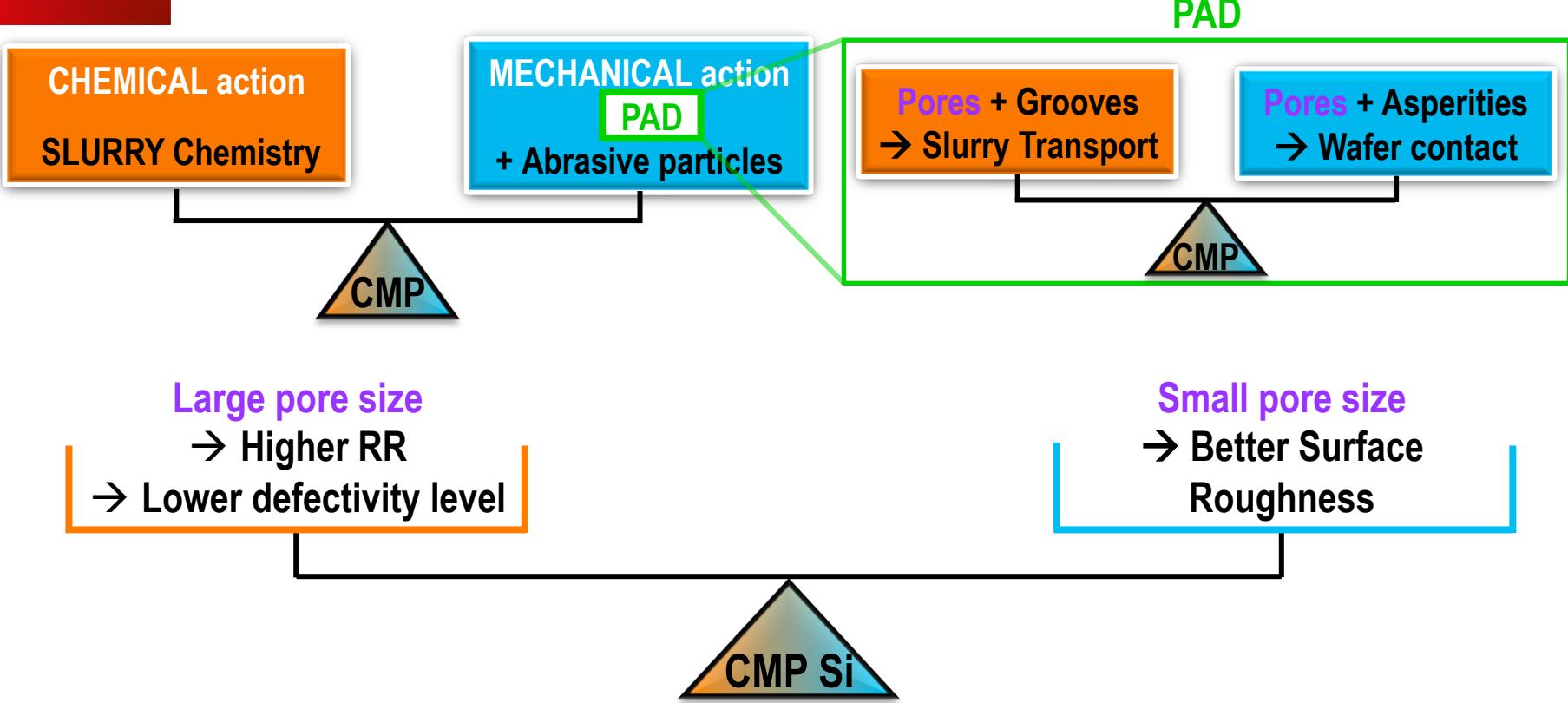
Increasing Open Pad Texture Increase RR and Decrease Defectivity Level

Si Wafer Quality Surface & Pad Texture Open



Chemical / Mechanical Balance in Si CMP Can Be Managed Through Pad Microstructure

Conclusion



Chemical/Mechanical Balance Management through Pad Microstructure Advanced Pad & Advanced Wafer Characterizations:

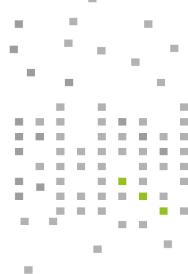
Better Understanding of Roughness Transfer from Pad to Wafer
Achieve Better CMP Performance



Thank you for your attention

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RF

