Post CMP Cleaning Conference @ SPCC2017

Post CMP Surface Preparation in sub 10 nm Devices

March 27, 2017
Jin-Goo Park

Department of Materials Engineering,
Hanyang University ERICA, Ansan, 15588, KOREA

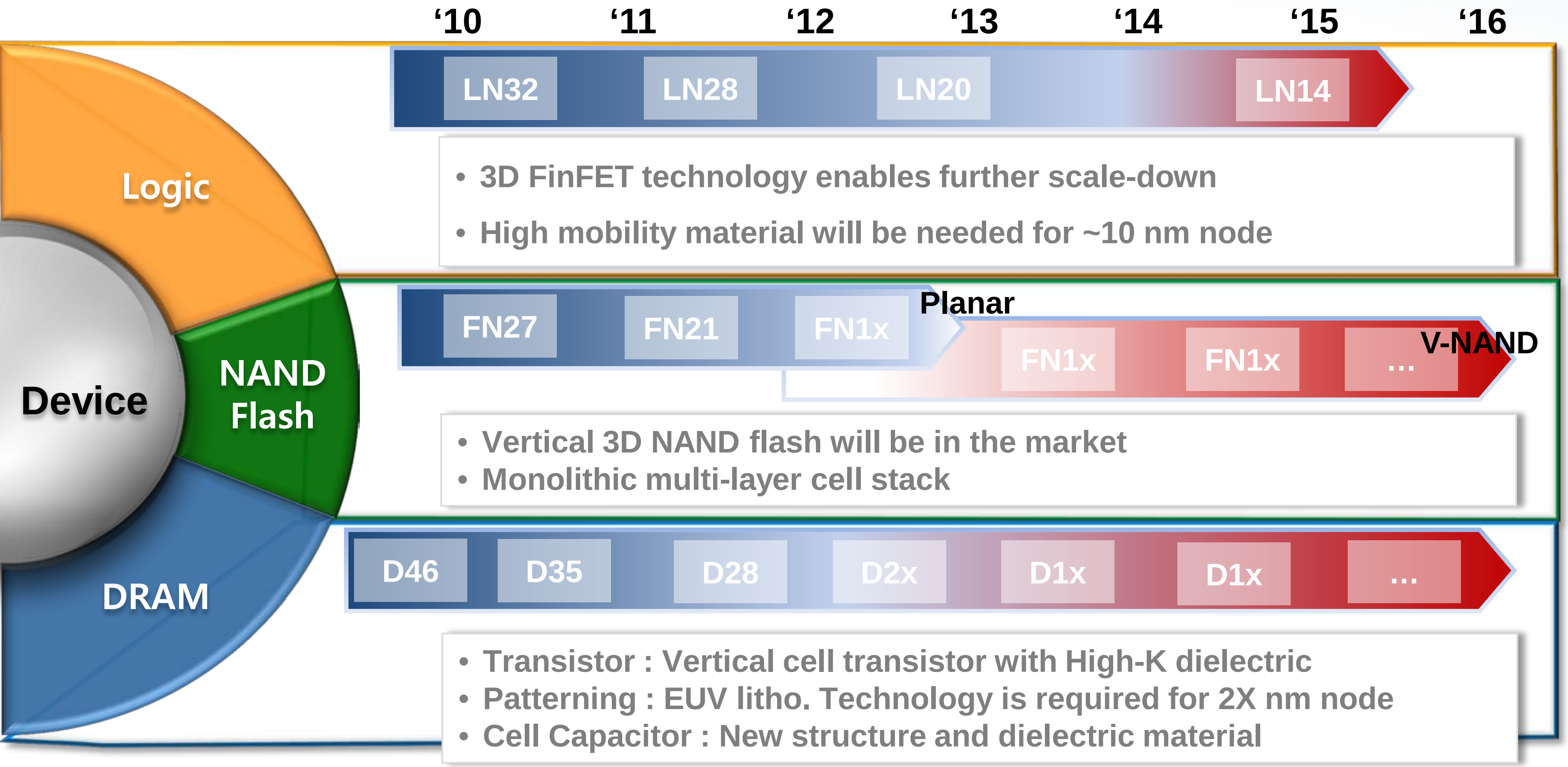
01 Challenges in surface preparation

- Research trend in cleaning technology
- Lesson learned from current cleaning technology

02 Challenges in post CMP surface preparation

- New paradigm in CMP process
- Current post CMP cleaning process
- New direction

Device Technology Roadmap

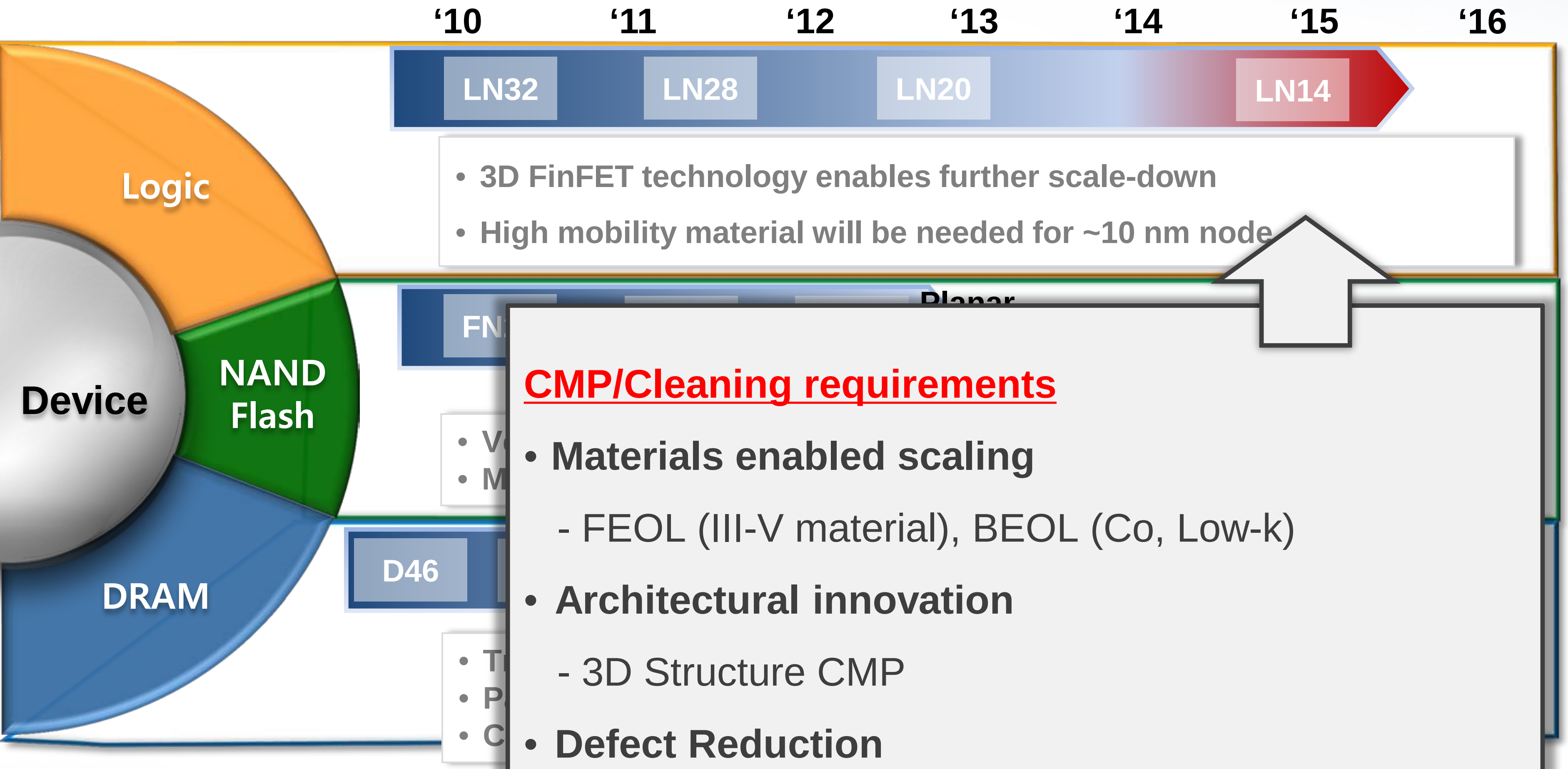


- 3D FinFET technology enables further scale-down
- High mobility material will be needed for ~10 nm node

- Vertical 3D NAND flash will be in the market
- Monolithic multi-layer cell stack

- Transistor : Vertical cell transistor with High-K dielectric
- Patterning : EUV litho. Technology is required for 2X nm node
- Cell Capacitor : New structure and dielectric material

Device Technology Roadmap

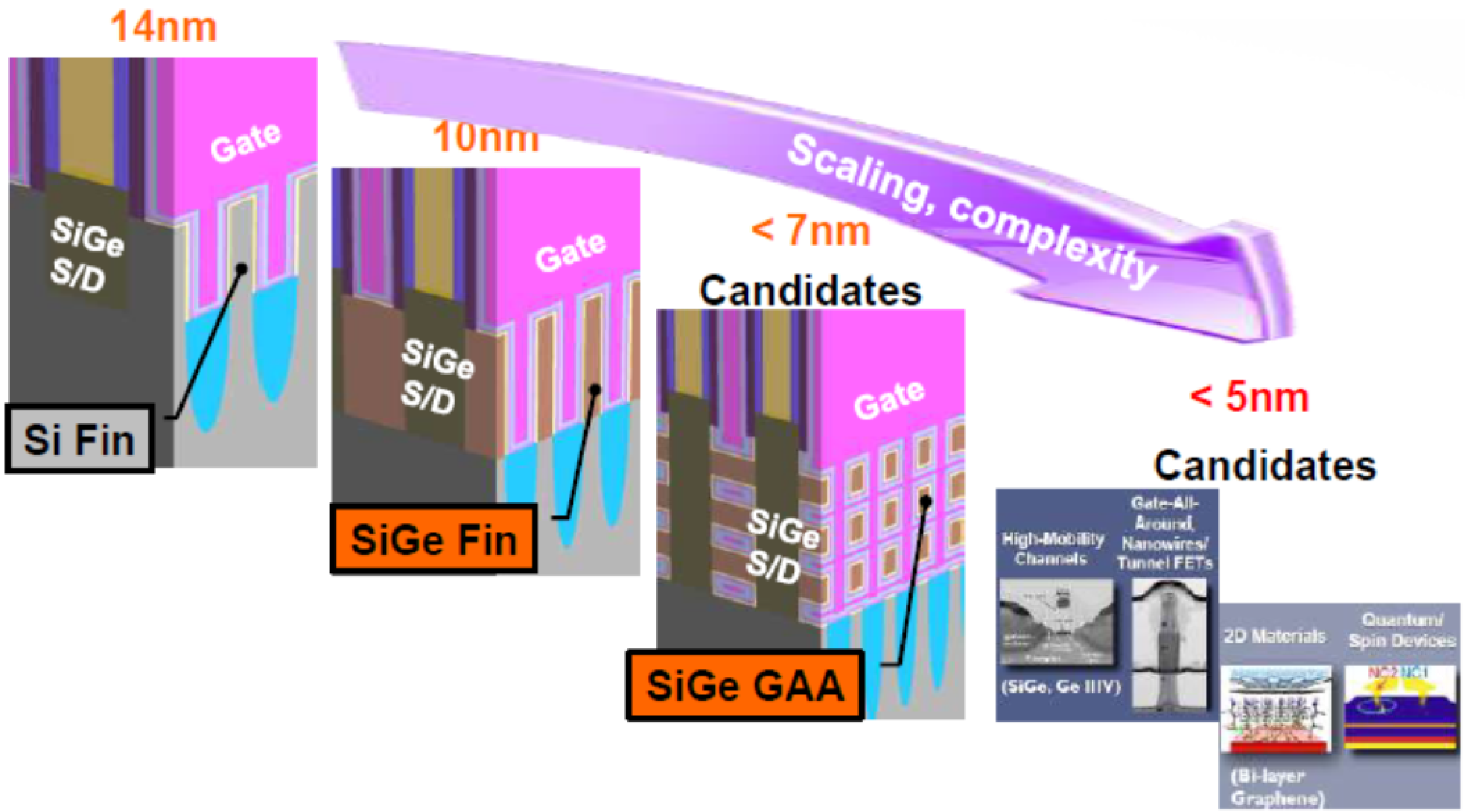


- 3D FinFET technology enables further scale-down
- High mobility material will be needed for ~10 nm node

CMP/Cleaning requirements

- **Materials enabled scaling**
  - FEOL (III-V material), BEOL (Co, Low-k)
- **Architectural innovation**
  - 3D Structure CMP
- **Defect Reduction**
  - Nano Sized Slurry, CVD Pad conditioner, Soft Pad, PVA brushes …

Logic Device Roadmap

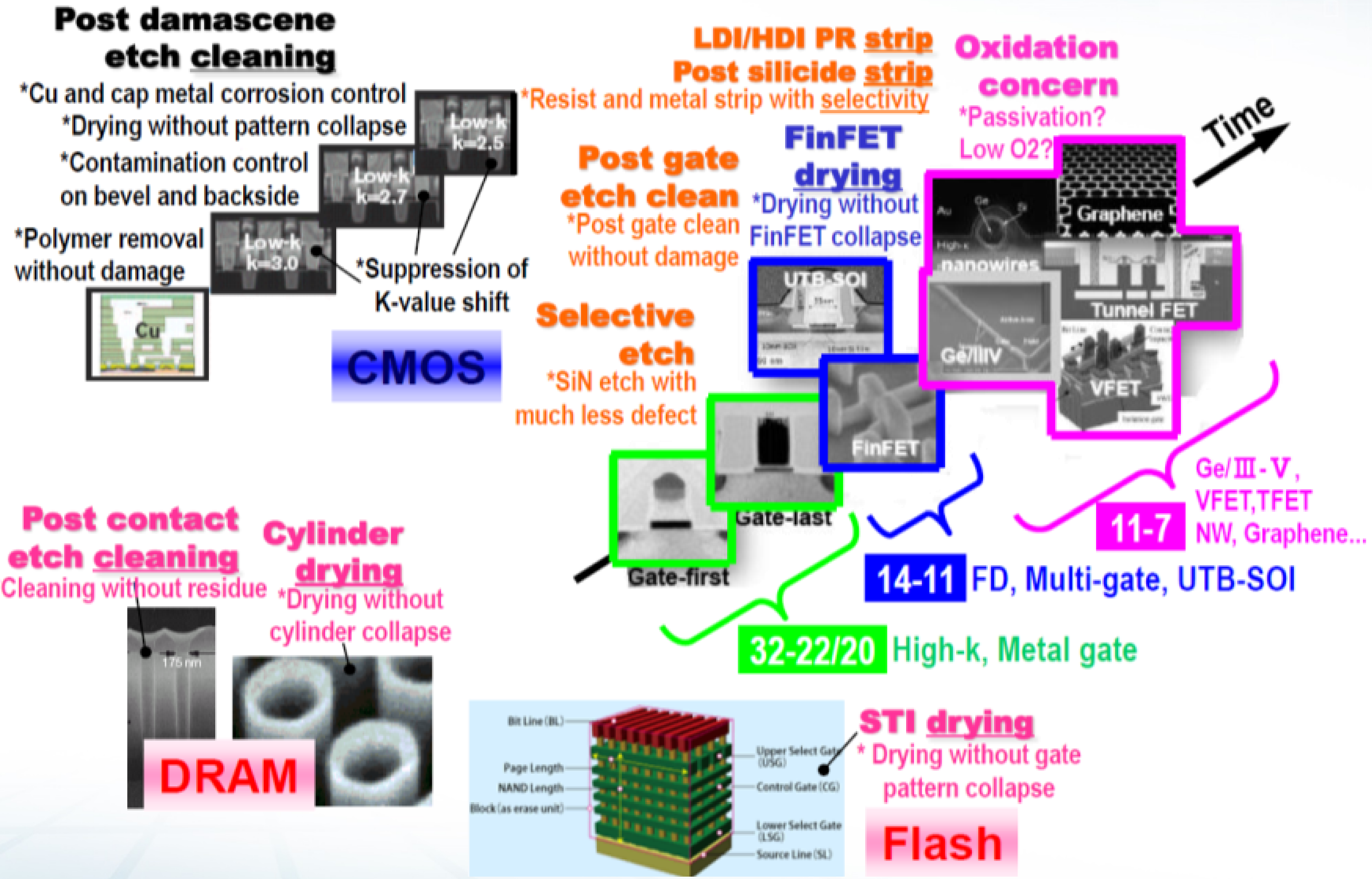


Courtesy of imec

- Scaling and structures are more complex
- Damage-free particle removal much more important

Screen, MRS 2016

Devices Cleaning Challenges



Post damascene etch cleaning

*Cu and cap metal corrosion control

*Drying without pattern collapse

*Contamination control on bevel and backside

*Polymer removal without damage

*Suppression of K-value shift

CMOS

LDI/HDI PR strip
Post silicide strip

*Resist and metal strip with selectivity

Oxidation concern

*Passivation? Low O2?

Post gate etch clean

*Post gate clean without damage

FinFET drying

*Drying without FinFET collapse

Selective etch

*SiN etch with much less defect

11-7 Ge/III-V, VFET,TFET NW, Graphene...

14-11 FD, Multi-gate, UTB-SOI

32-22/20 High-k, Metal gate

Post contact etch cleaning

*Cleaning without residue

Cylinder drying

*Drying without cylinder collapse

DRAM

STI drying

* Drying without gate pattern collapse

Flash

J. Snow, “Advanced Particle Removal Techniques for ≤20nm Device Node”, SPCC (2012)

Next Generation Surface Preparation

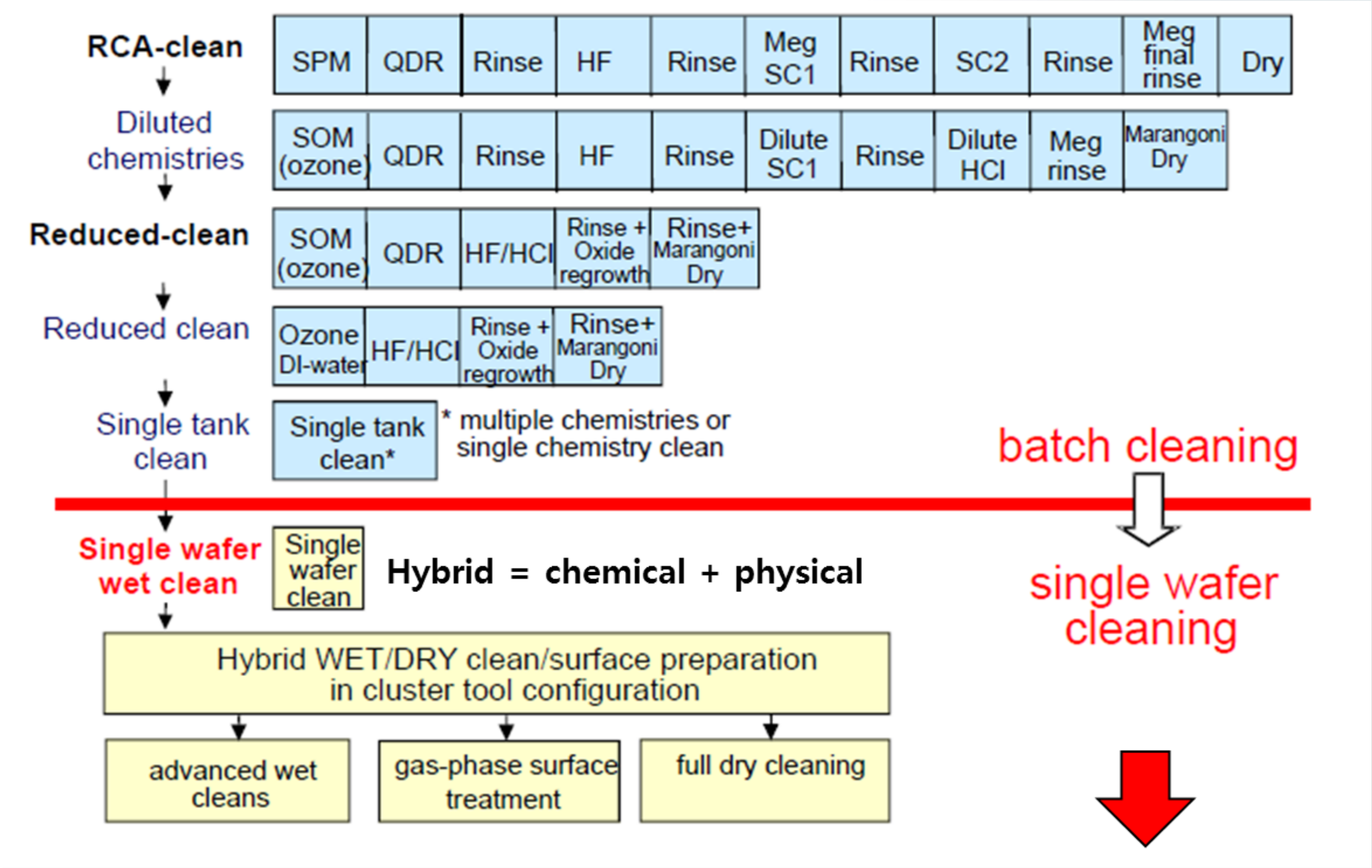
Issues

- Nanometer Feature Size
- New Materials
- Nanometer Thin Film
- Single Wafer Cleaning
- CMP Process
- EUVL Process
- 3D Device
- High Aspect Ratio

Challenges

- Clean without Etching
  - *Non RCA (H_2O_2 based) Chemistry*
- Clean without Pattern Damage
  - *No Megasonics and Brushes*
- CMP Induced Defects
(nano particles and organic defects)
- Zero Defect on EUVL Mask/Pellicle
- Drying without pattern leaning
- High selectivity dry etching/cleaning

Cleaning sequences: roadmap



RCA-clean	SPM	QDR	Rinse	HF	Rinse	Meg SC1	Rinse	SC2	Rinse	Meg final rinse	Dry
Diluted chemistries	SOM (ozone)	QDR	Rinse	HF	Rinse	Dilute SC1	Rinse	Dilute HCl	Meg rinse	Marangoni Dry	
Reduced-clean	SOM (ozone)	QDR	HF/HCl	Rinse + Oxide regrowth	Rinse+ Marangoni Dry						
Reduced clean	Ozone DI-water	HF/HCl	Rinse + Oxide regrowth	Rinse+ Marangoni Dry							
Single tank clean	Single tank clean*										
Single wafer wet clean	Single wafer clean										

* multiple chemistries or single chemistry clean

batch cleaning

single wafer cleaning

Hybrid = chemical + physical

Hybrid WET/DRY clean/surface preparation in cluster tool configuration

- advanced wet cleans
- gas-phase surface treatment
- full dry cleaning

No Material loss and Damage Free Cleaning???

Rita Vos and Paul Mertens, "General aspects of cleaning Sequences", UCPSS (2010)

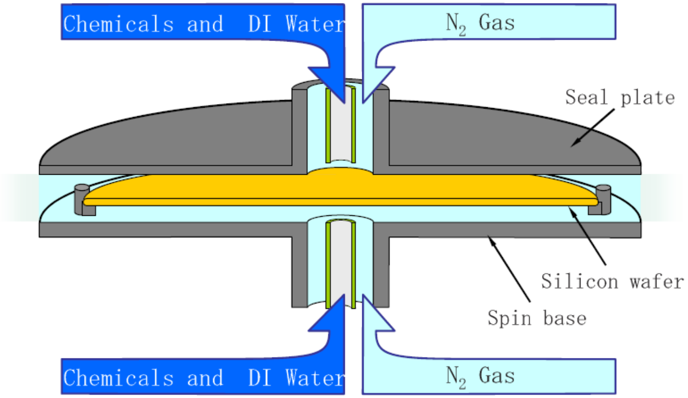
Traditional Wafer Cleaning Chemicals and Technology

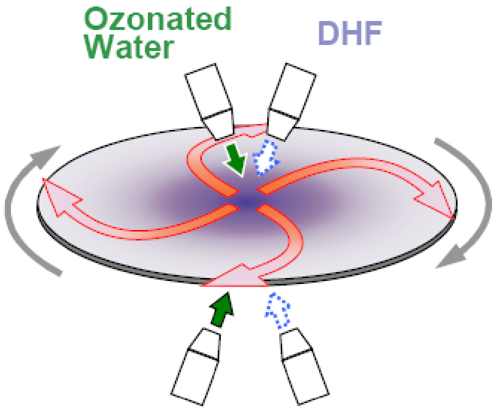
- SC-1($NH_4OH+H_2O_2+H_2O=1:1:5$ at 80 ~ 90°C)
  - Particles and organic contamination removal
- SC-2($HCl+H_2O_2+H_2O=1:1:5$) at 80 ~ 90 °C)
  - Trace and Noble Metal removal
- Piranha($H_2SO_4:H_2O_2=4:1$ at 9
  - Organic Contamination rem
- HF (+ H_2O_2) : Last wet cleani
  - HF : Native oxide and H_2O_2

Single Wafer Cleaning Technology

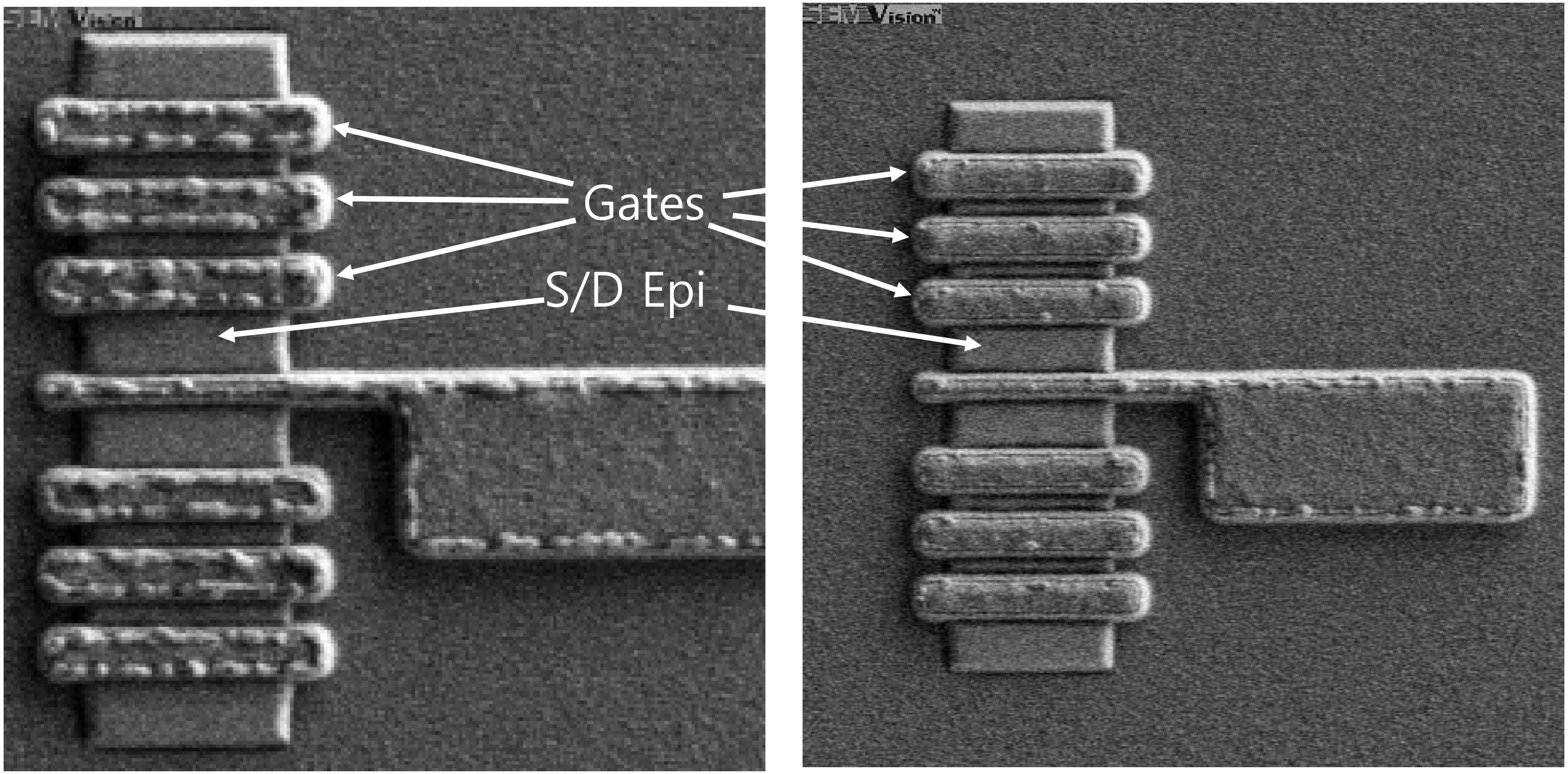
- Single wafer offers significant advantages over batch processes
  - Reduces power uniformity problem from a 3-dimensional to a 2-dimensional geometry

  + usual single wafer benefits:
  - Defect control (cross-contamination, etc.)
  - Chemical control & selectivity
  - Backside isolation





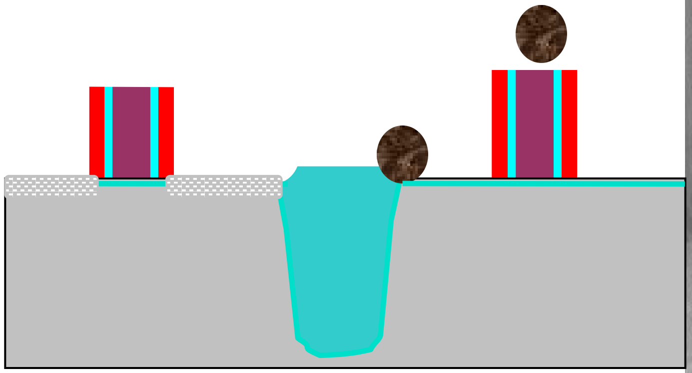
Single Wafer vs. Wet Bench Cleans

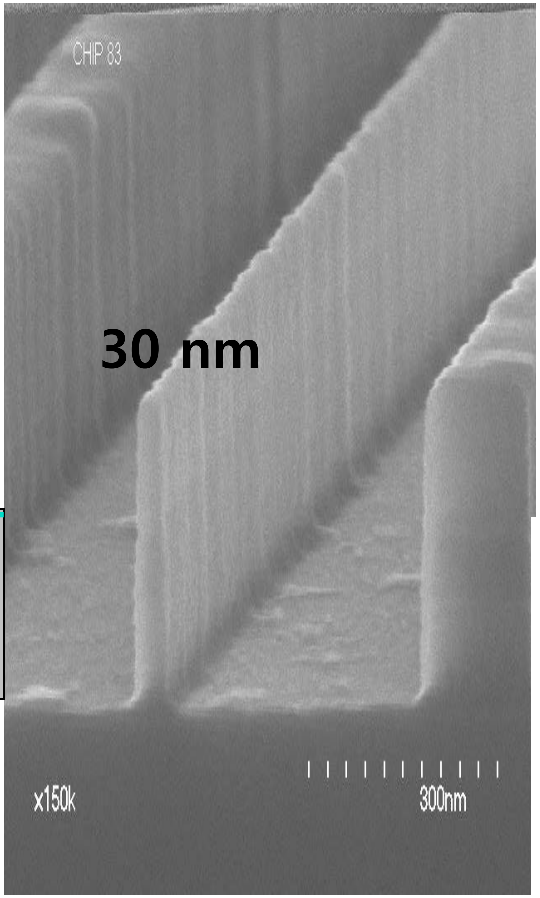


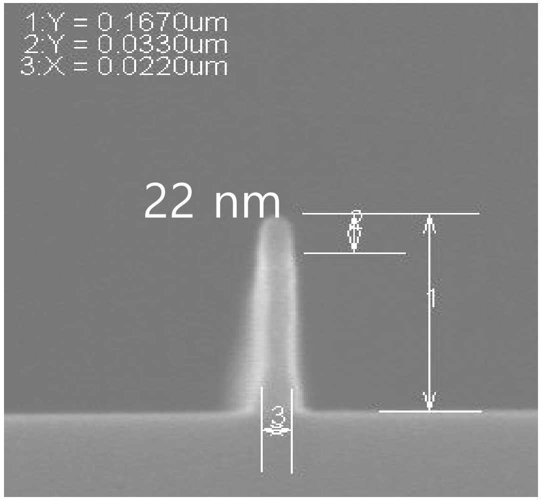
All Cleans on Wet Bench
⇒ Overetched Hard Mask

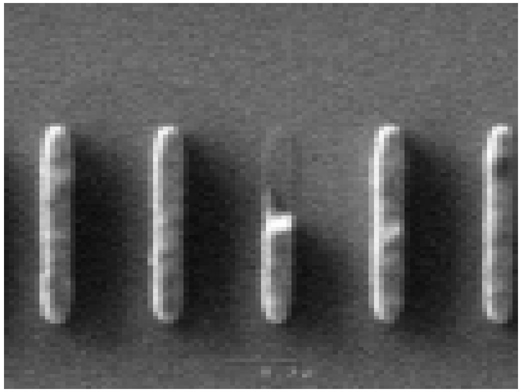
All Single Wafer Cleans
⇒ Reduced overetch
⇒ Improved Selectivity

Cleaning of Fragile Structures



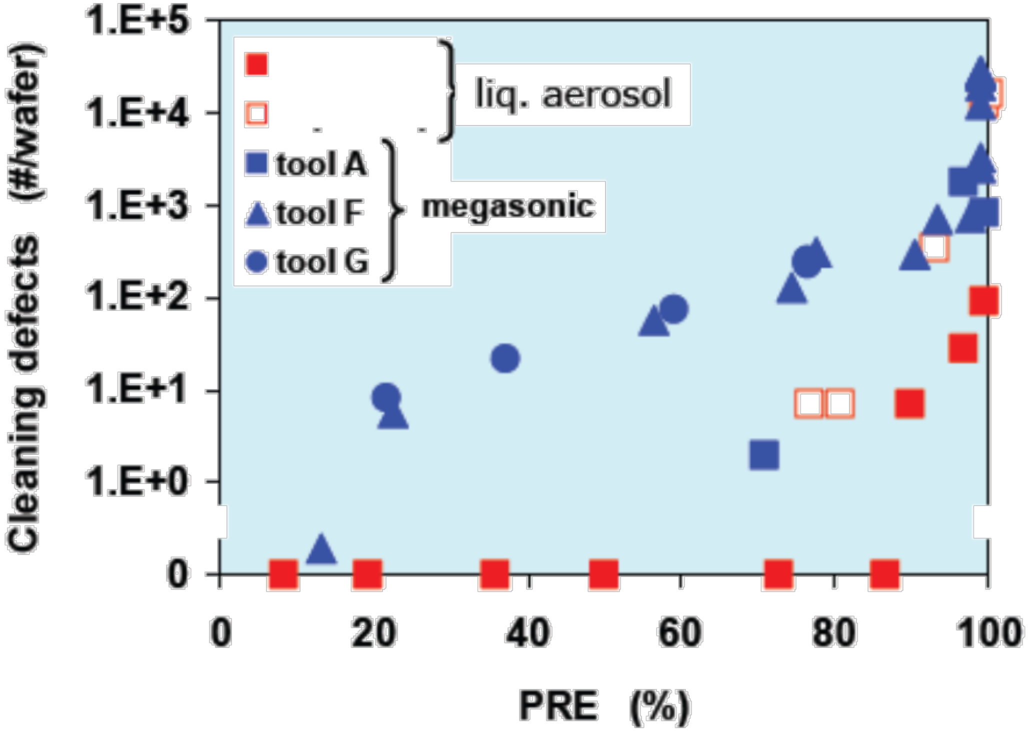






Cleaning without damages

Damage to poly-gate-stack lines vs. Part. Rem. Eff. 78-nm SiO_2



all physical cleaning methods yield higher PRE at expense of increased damage

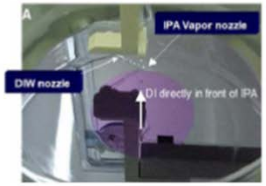
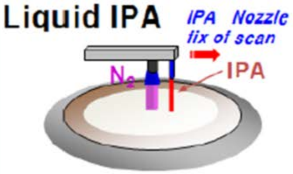
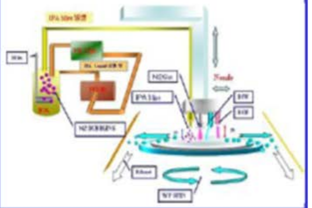
[G. Vereecke et al, UCPSS 2006]

first sight: liquid aerosol gives best performance, but:

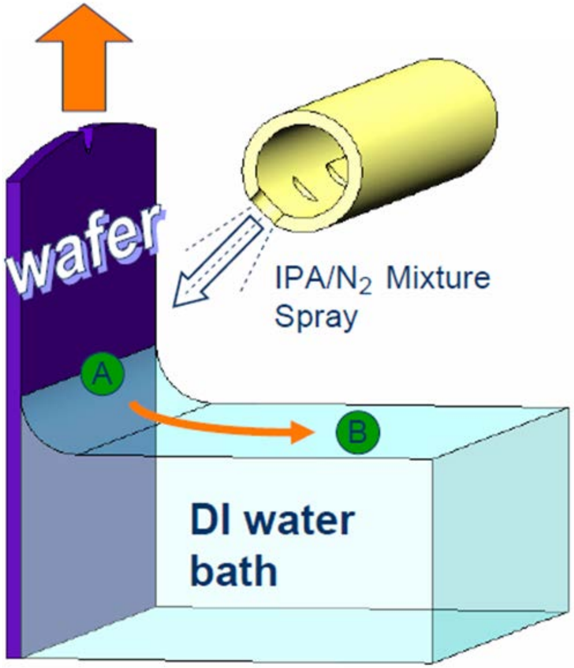
- lower performance of megasonic is attributed to non-uniformity,
  ➔ may be overcome by appropriate engineering? other: conc. diss. gas Xc
- behaviour for further scaled features, particles remains to be tested
- cleaning inside vias and trenches needs to be compared

Wafer Drying Technology

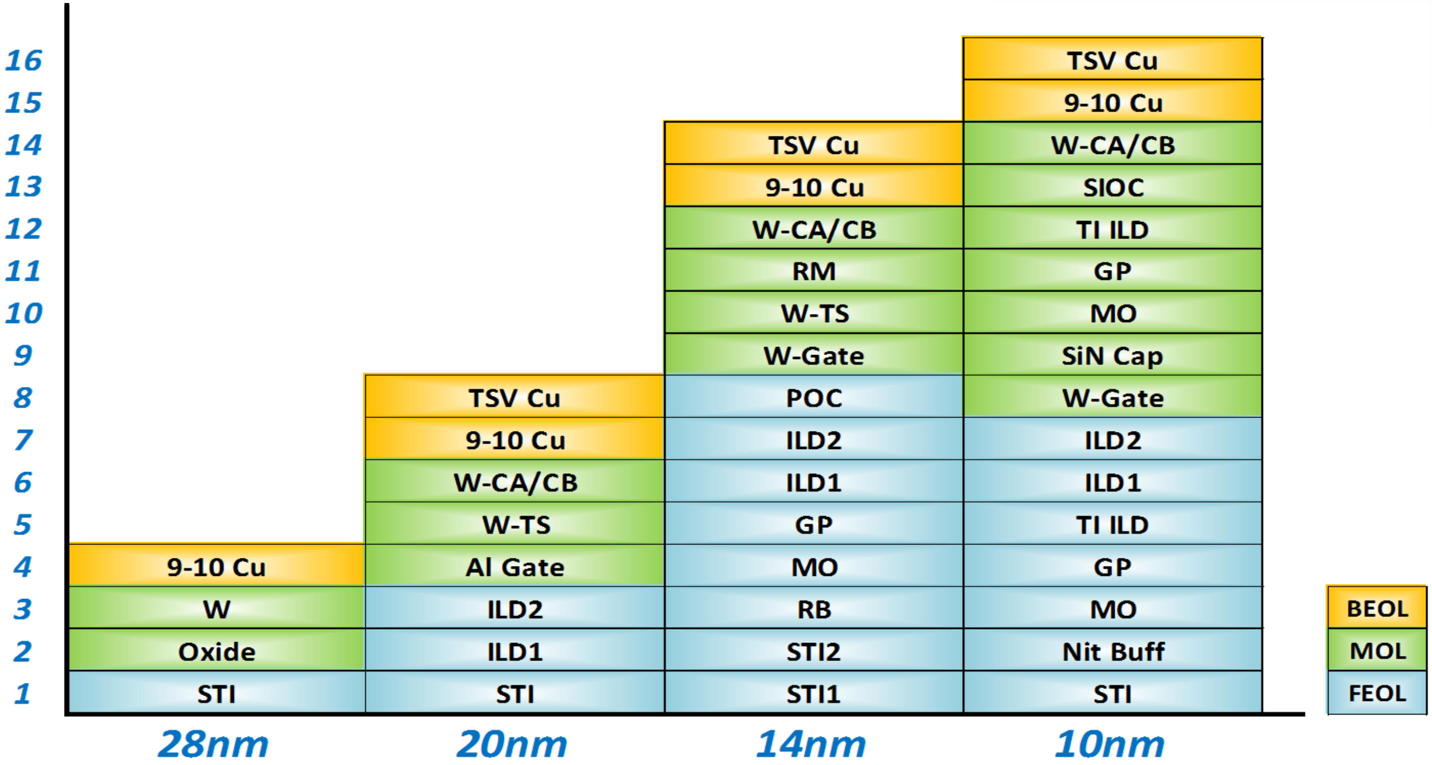
Spin dryer –DI water, liquid IPA, vapor IPA, hot IPA

	A	B	C
Drying	IPA vapor (Rotagoni, spin)	IPA Liquid (Spin)	IPA Vapor (spin)
			
Dryer	Goldfinger	TEL etc	NMD Dryer
	-Rotational force + marangoni force	-Liquid IPA : low surface tension -IPA Nozzle fix or scan to wafer edge	-IPA vapor -Controllable of IPA eject angle

Marangoni IPA dryer



CMP Challenges in 10 nm/7 nm



	28nm	20nm	14nm	10nm
16				TSV Cu
15				9-10 Cu
14			TSV Cu	W-CA/CB
13			9-10 Cu	SIOC
12			W-CA/CB	TI ILD
11			RM	GP
10			W-TS	MO
9			W-Gate	SiN Cap
8		TSV Cu	POC	W-Gate
7		9-10 Cu	ILD2	ILD2
6		W-CA/CB	ILD1	ILD1
5		W-TS	GP	TI ILD
4	9-10 Cu	Al Gate	MO	GP
3	W	ILD2	RB	MO
2	Oxide	ILD1	STI2	Nit Buff
1	STI	STI	STI1	STI

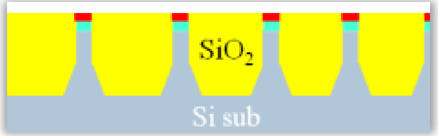
- Number of CMP steps doubled from 28nm to 10nm node in order to enable new integration schemes such as replacement metal gate and self-aligned contact.
  - ~ 75% of the increase is in MOL due to the complexity of contact module.
- New CMP processes such as Co, Cap SiN and SiOC CMP in MOL

J. Han, CSTIC, 2016

CMP Process for 3D FinFET -FEOL

- Critical CMP step in FEOP for sub-28 nm Replacement Metal Gate application (RMG) FinFET technology have been described

STI CMP for bulk FinFET

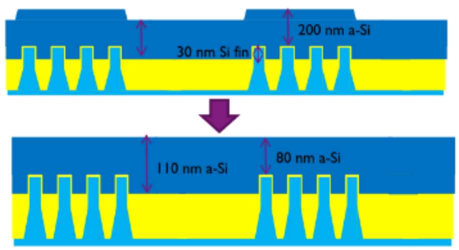


Spec on SiN :
< 2nm variation WID/WIW

Fin formation

Gate deposition

Gate Planarization



Thickness on Fin and on Field :
<5 nm WID/WIW

Gate patterning

Ext. / HALO implant

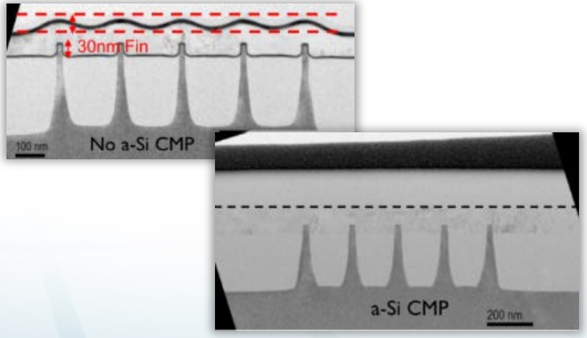
Spacers formation

HDD Si epi

HDD implantation

Anneal

CESL and ILD0 deposition



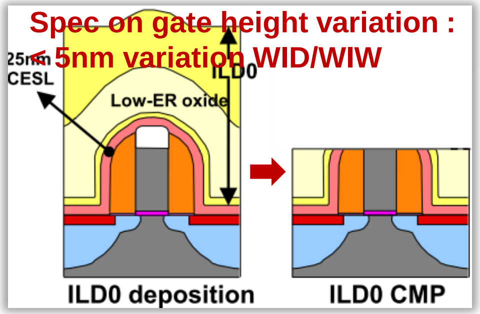
Poly-open or ILD0 CMP

Dummy gate removal

Dummy dielectric removal

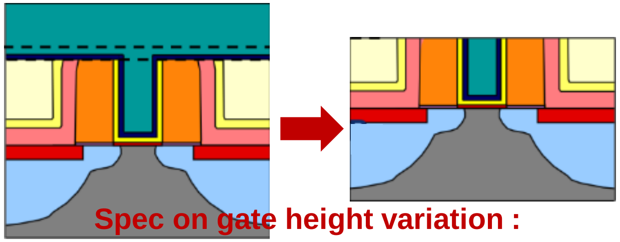
IL-SiO_2/HfO_2 deposition

WF MG + Fill-in MG deposition



Spec on gate height variation :
< 5nm variation WID/WIW

MG CMP



Spec on gate height variation :
< 5nm variation WID/WIW

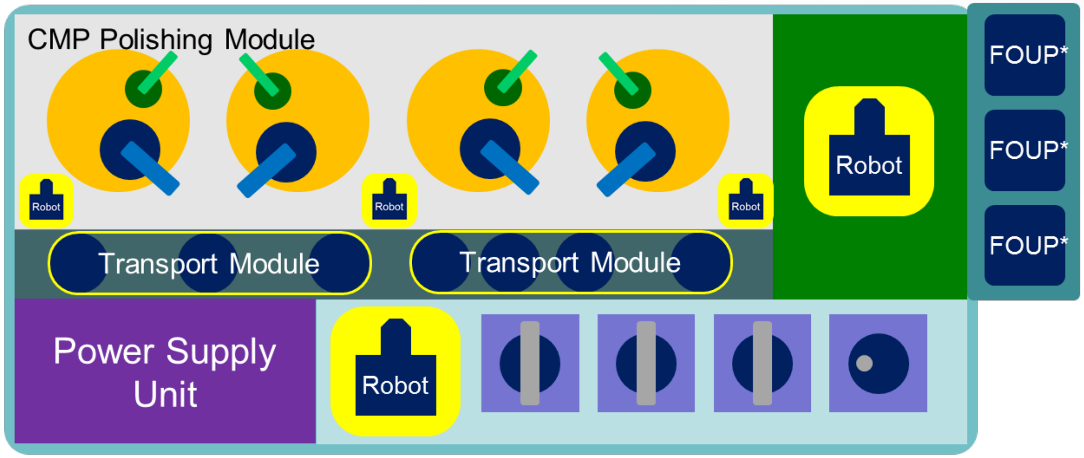
- Each CMP step has tight SPEC's in terms of WID and WIW uniformity control
- Continuous improvement ongoing towards smaller technology nodes

*K. Devriendt, P. Ong, ICPT2012, *K. Devriendt, K. Kellens, A. Veloso, R. Athimulam, ICPT2011, p536

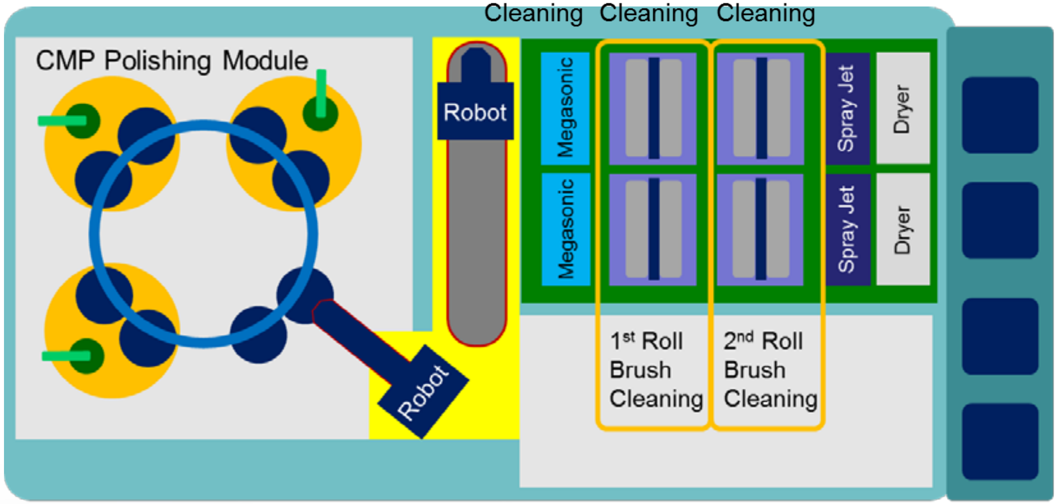
How do we clean polished wafers?

PVA Brushes!!

(*FOUP = Front Opening Unified Pod)



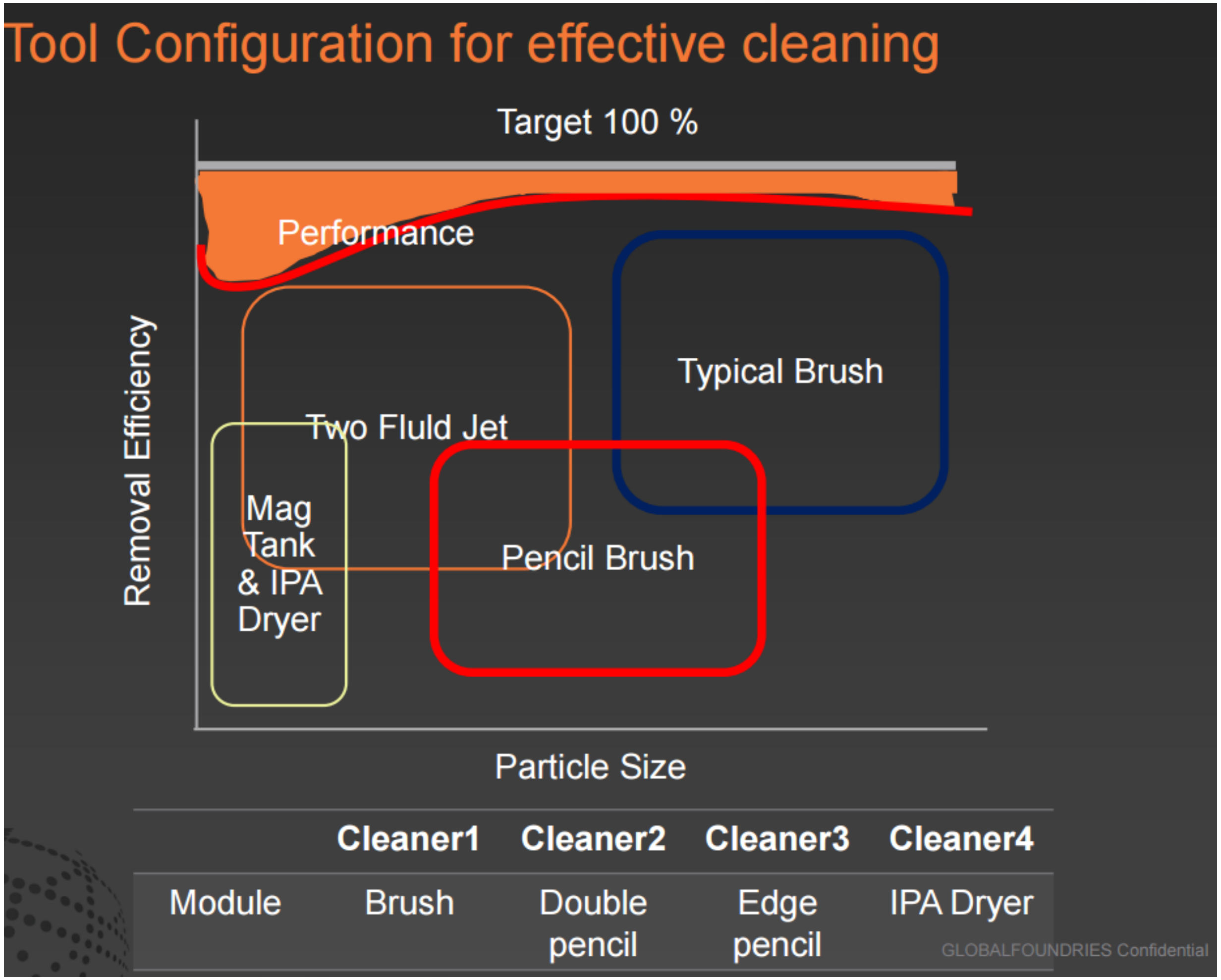
< "E" CMP & P-CMP Tool >



< "A" CMP & P-CMP Tool>

Cassette Line

Nano Particle Removal in Post CMP Cleaning



Tool Configuration for effective cleaning

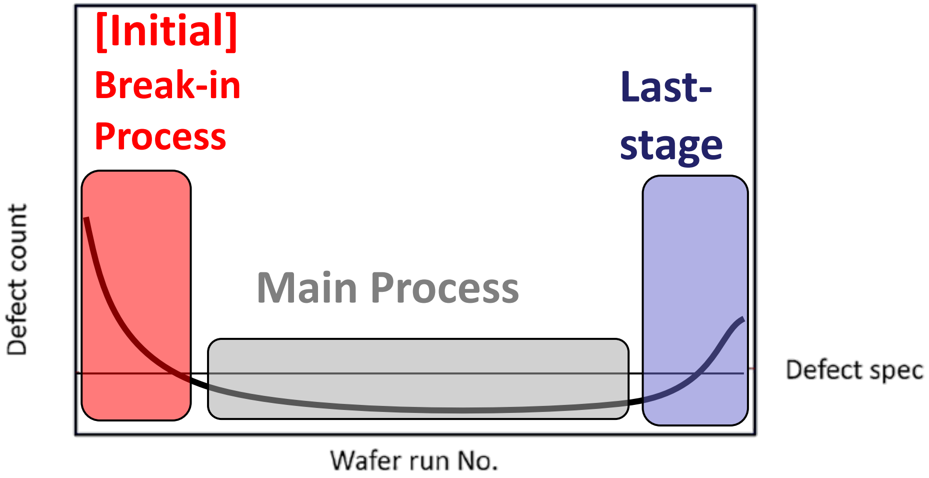
	Cleaner1	Cleaner2	Cleaner3	Cleaner4
Module	Brush	Double pencil	Edge pencil	IPA Dryer

- **Typical Brush (Large Particle) + Pencil Brush (Middle Particle)**

GF, SPCC 2015

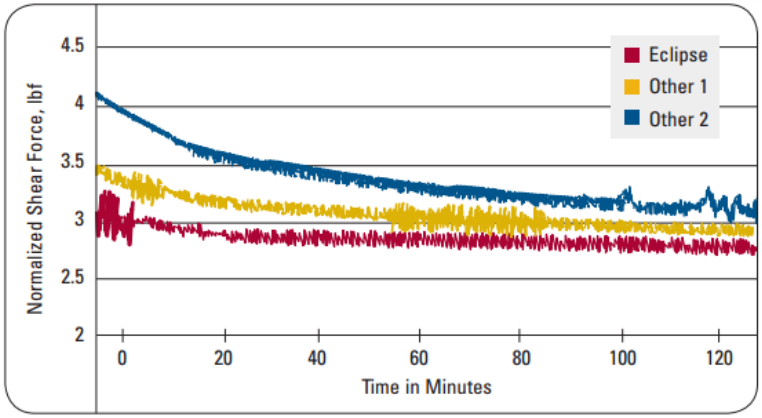
Defect Level of PVA Brush's Stage

< Defect count vs. Time>



- Initial > Last-stage >> Main Process

< Shear Force Vs. Time>

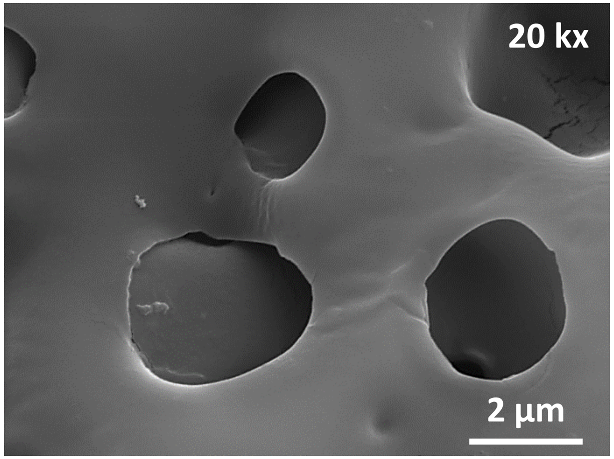


*Ref: ITW Rippey

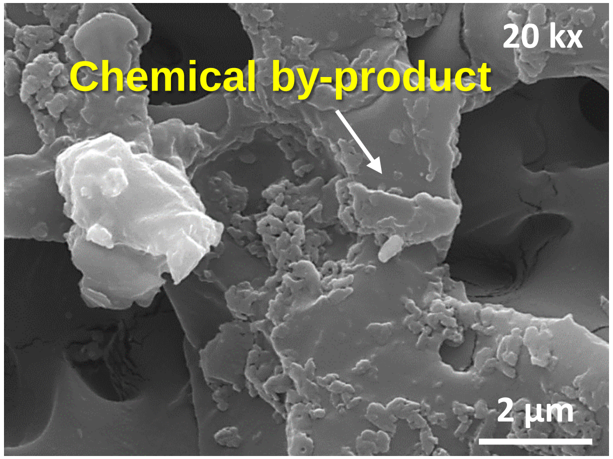
- **Defect count is increased** by brush cleaning in long run process.
- **Shear force is decreased** by brush cleaning in long run process.
- **PVA brush cleaning performance decreases as a function of process time**.

FE-SEM Analysis of Fully-Used PVA Brush

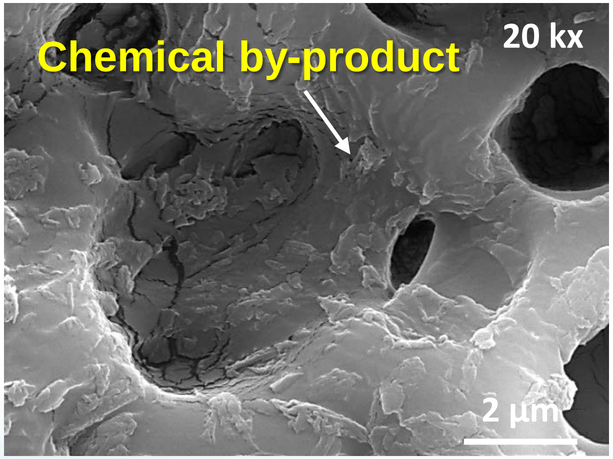
❖ **New Brush**



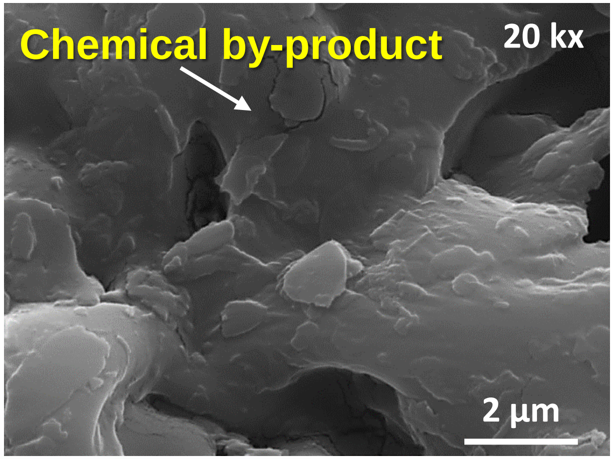
❖ ***Post Tungsten CMP (Silica) – DHF***



❖ ***Post Oxide CMP (Silica)***
– SC-1 Cleaning



❖ ***Post Oxide CMP (Silica)***
– DHF



❖ ***Post Oxide CMP (Ceria)***
– DHF

- **Different types of slurry and cleaning chemistry affect contamination of brush surface.**

Brush Treatment Methods with Different Chemicals

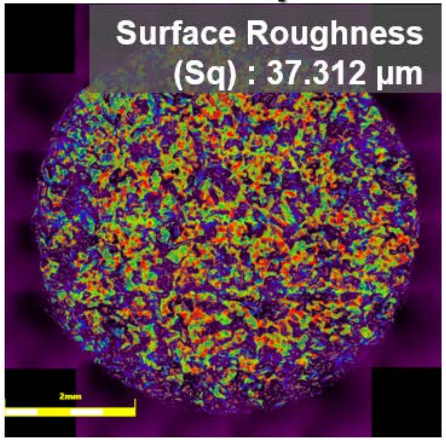
#	Method	Solution	pH
1	Dipping (24 Hr)	DIW	7
2		DHF (0.9:100 = HF:DIW)	3.1
3		SC-1 (1:2:40 = NH_4OH:H_2O_2:DIW)	10.2
4	Scrubbing (12 Hr)	DIW	7
5		DHF (0.9:100 = HF:DIW)	3.1
6		SC-1 (1:2:40 = NH_4OH:H_2O_2:DIW)	10.2

← **Reference Condition**

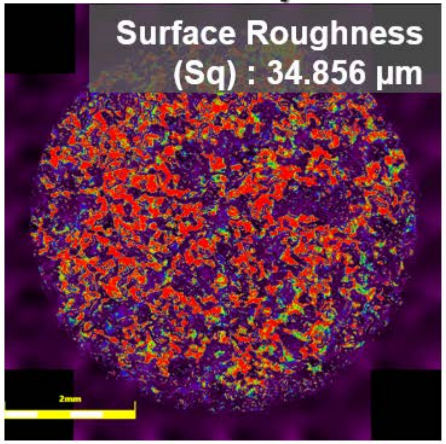
- **2 Types of Method : Dipping / Scrubbing**
- **3 Types of Solution : DIW / SC-1 / DHF**

3D-Profiler Analysis of Chemical Treated PVA Brushes

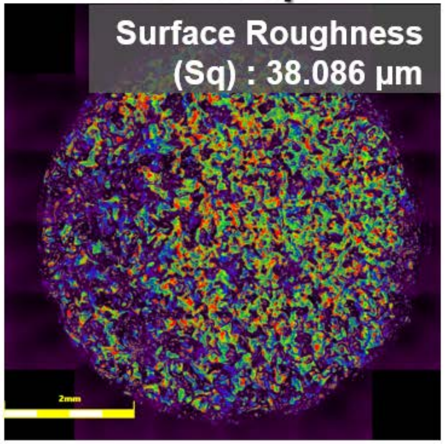
DIW Dip



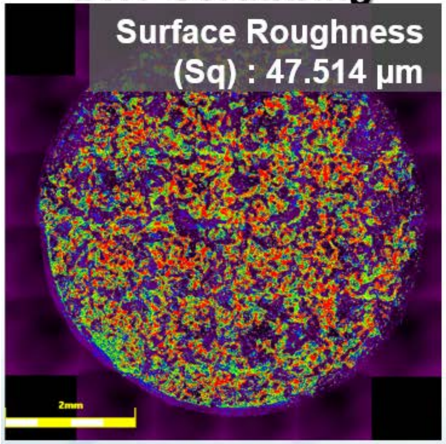
DHF Dip



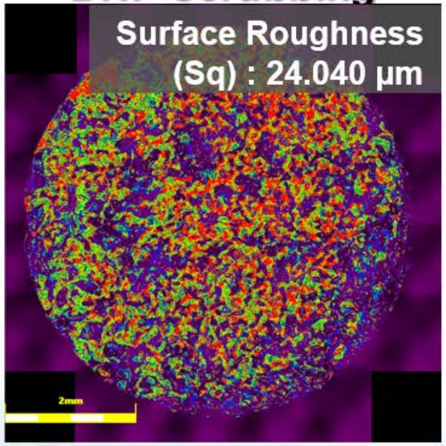
SC-1 Dip



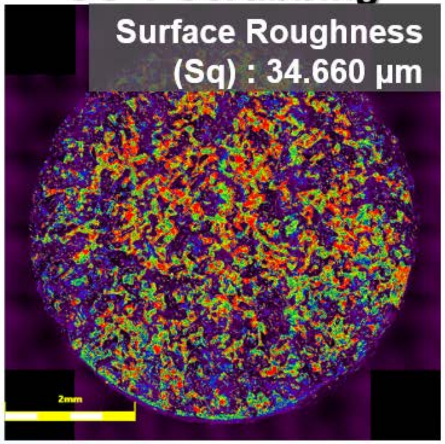
DIW Scrubbing



DHF Scrubbing



SC-1 Scrubbing

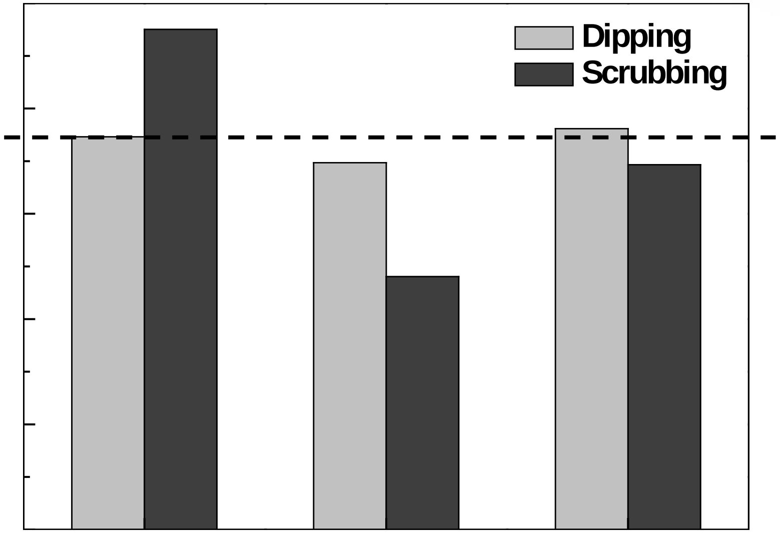


- **DHF scrubbed PVA brush shows flattened surface.**
- **SC-1 scrubbed PVA brush shows rough surface.**

$$Sq = \sqrt{\iint_{a} (Z(x, y))^2 \, dxdy}$$

3D-Profiler Analysis of Chemical Treated PVA Brushes

❖ Analyzed Surface Roughness of Various Chemical Treated PVA Brushes

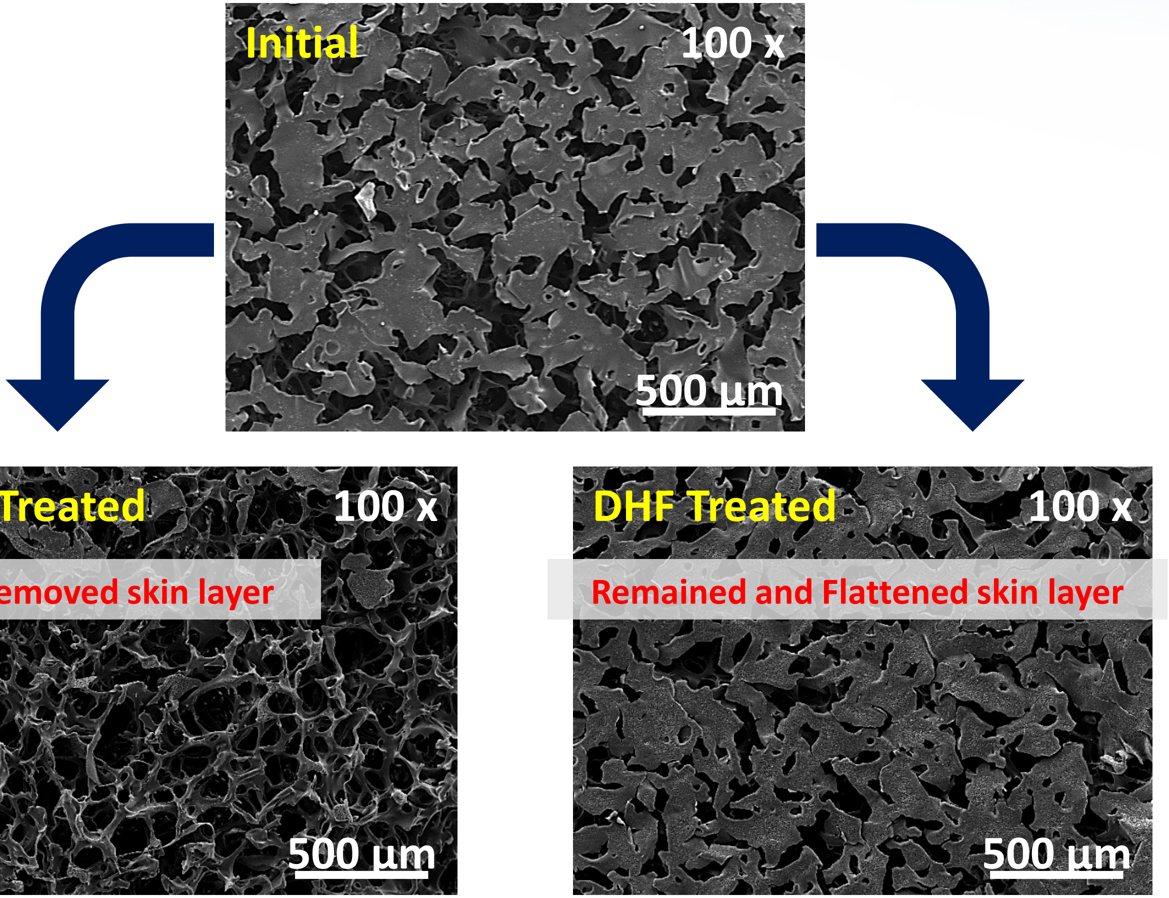


- **All dipped brushes show the similar** morphology and surface roughness.
- **The scrubbed brushes show significant change** in morphology and surface roughness.

➡ **It will affect the change of real contact area** between brush and particles on wafer.

- **DHF scrubbed PVA brush shows flattened surface with the lowest surface roughness.**

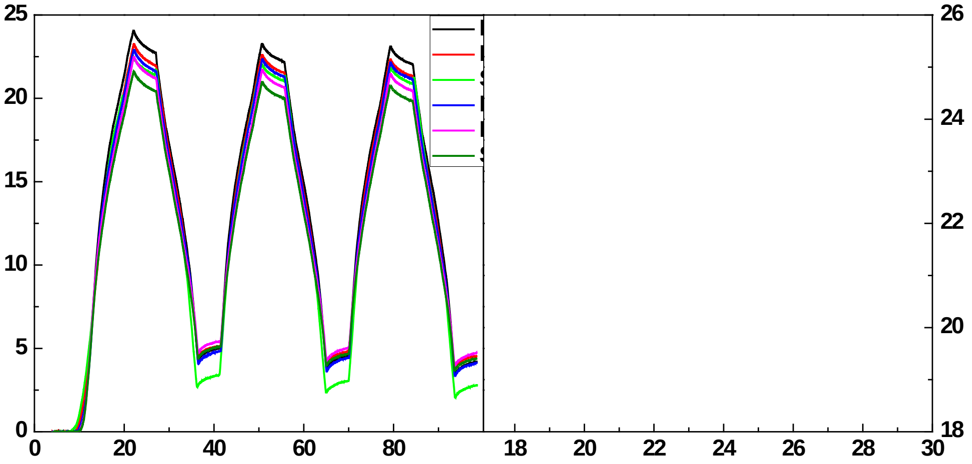
FE-SEM Analysis of Chemical Treated PVA Brushes



- **SC-1 treated brush shows the removed skin layer.**
- **DHF treated brush shows remained and flattened skin layer.**

➡ **It will affect the final cleaning performance on wafers.**

Compress Stress Analysis of Chemical Treated PVA Brushes



#	Method	Cleaning sol.	Maximum Load (gf)	Compressive Strength (gf/mm^2)
1	Dipping	DIW	24.061	0.962
2		DHF	23.266	0.931
3		SC-1	22.550	0.902
4	Scrubbing	DIW	22.903	0.916
5		DHF	22.484	0.899
6		SC-1	21.614	0.865

(a) (b) (c)

(a) compressive stress measurement of various chemical treated brushes, (b) its magnified region, (c) compressive strength

- **A significant change of elastic property** was observed in **scrubbed brush** when compared to the chemical dipped brush.
- **The SC-1 treated brush showed more changes** in its compressive stress than DHF treated brush.

Effect of Brush Treatment Methods and Chemicals

	Dipping	Scrubbing		
		Overall	DHF	SC-1
Surface morphology	Similar	**Significant changes**	**Flattened**	**Rough**
Surface roughness value	Similar	**Significant changes**	**Lowest**	
Skin layer	Remained	**Significant changes**	Remained	**Removed**
Elastic property	Similar	**Significant changes**		**Lowest**

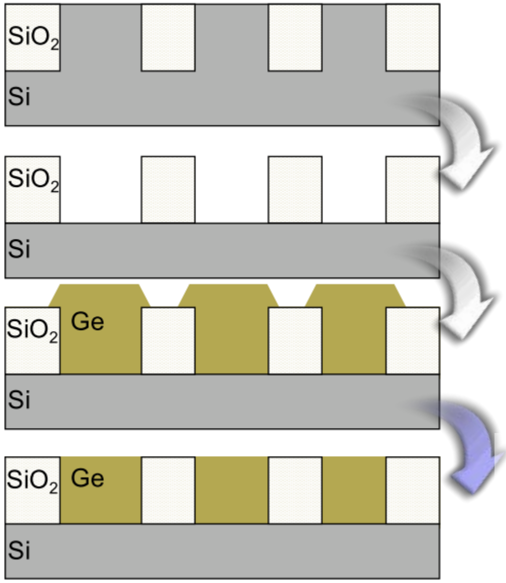
- **The scrubbed brushes show the significant changes in the morphology and surface roughness.**
- **The SC-1 treated brush shows more elastic and morphological changes than DHF treated brush.**

CMP Process for High Mobility Channel Materials

❖ **CMOS performance can be enhanced by using high-mobility channel materials**

- III/V materials (nMOS) : high electron mobility / Ge (pMOS) : high hole mobility

- The approach followed in this work is **Ge-STI approach**

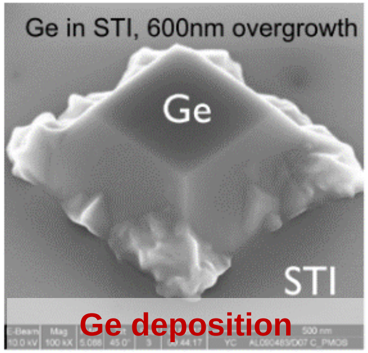


Standard STI on bulk Si wafer

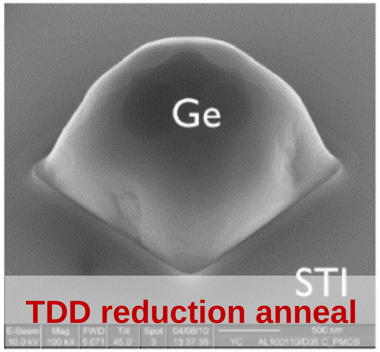
Selective Si recess etch

Selective epitaxial Ge growth on Si

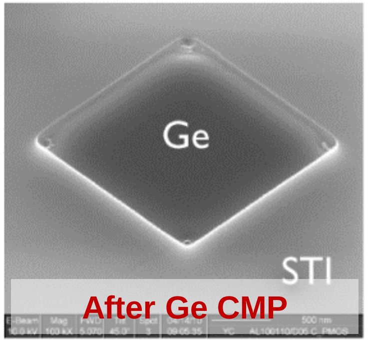
CMP of Ge stopping on SiO$_2$



Ge deposition



TDD reduction anneal



After Ge CMP

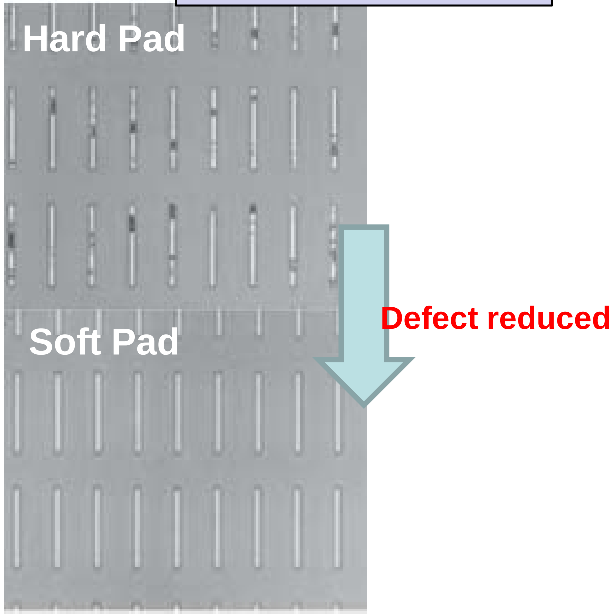
- **CMP requirement**
  - Good planarity
  - Low amount defects
  - Low surface roughness

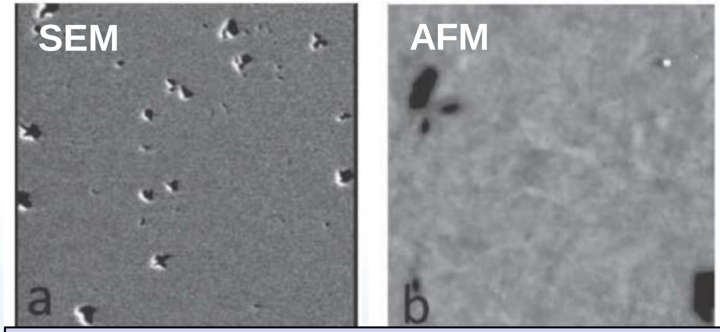
***P. Ong, C. Gillot, S. Ansar, B. Noller, Y. Li, L. Leunissen, ICPT2012, p23**
***P. Ong, L. Witters, ICPT2010, p69**

Low Defectivity III-V CMP Process

❖ Improving Defectivity for III-V CMP Processes for <10 nm Technology Nodes

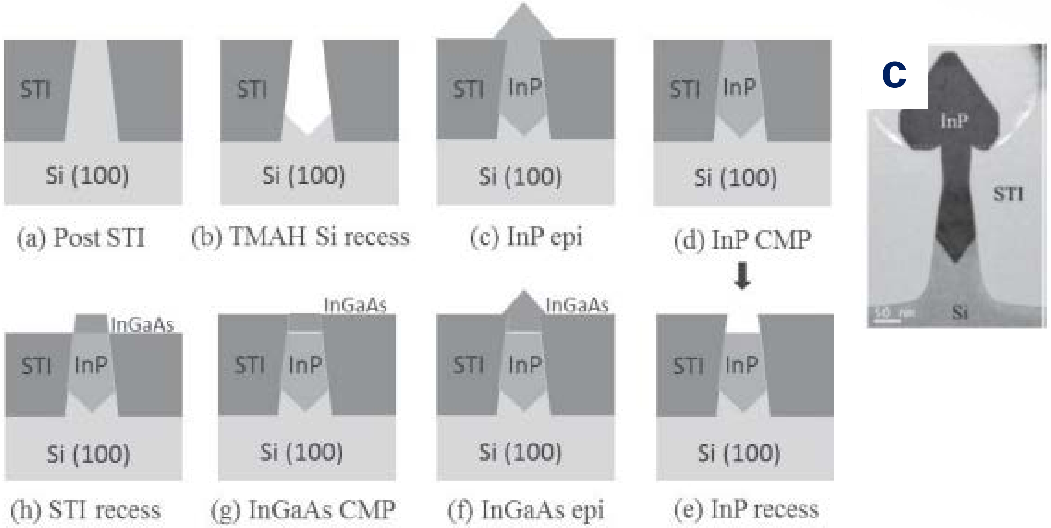
InP-filled structure





InGaAs surface post CMP using soft pad

Integration of III-V channels ART



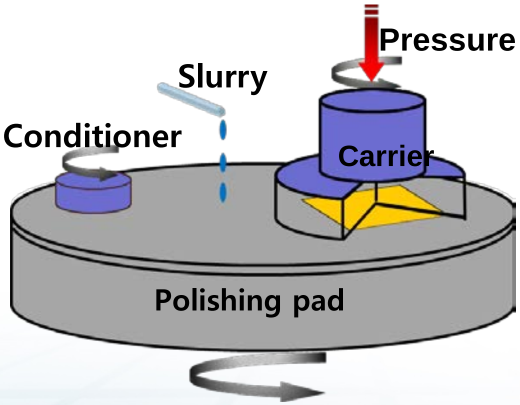
- InP in STI trenches can be removed by choosing the appropriate slurry/pad combination – Hard Pad < Soft Pad
- Good surface achieved by using soft pad
- Not yet optimized on defect control on polished III-V surfaces

*Lieve Teugels, Patrick Ong, Guillaume Boccardi, Niamh Waldron, ICPT2014, p15

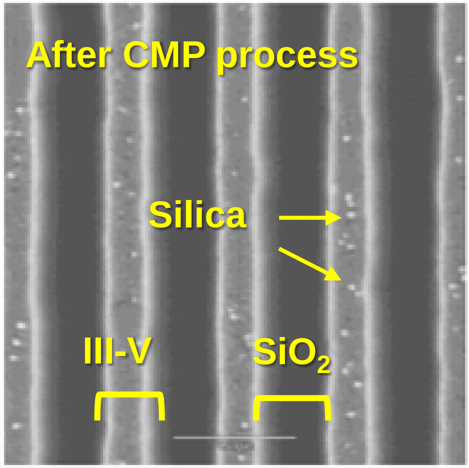
Post InGaAs CMP Cleaning

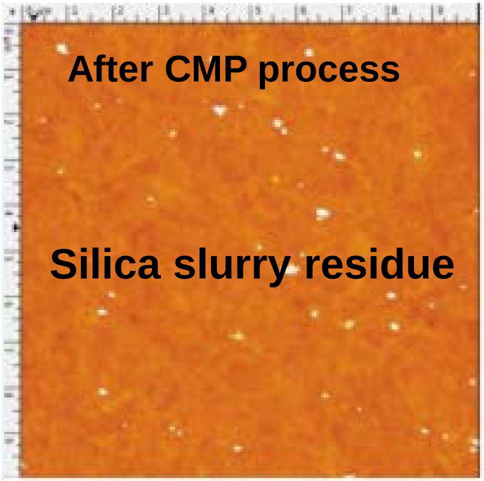
❖ Issues of III-V post CMP cleaning

- InGaAs CMP using silica slurry
- Silica slurry abrasives were not removed perfectly after post CMP cleaning
  - DIW megasonic followed by 2 brush steps with <1% diluted ammonia
- Need to selective cleaning of III-V surface
  - ✓ Chemical cleaning : etching, electro-repulsion
  - ✓ Physical cleaning



Post CMP cleaning

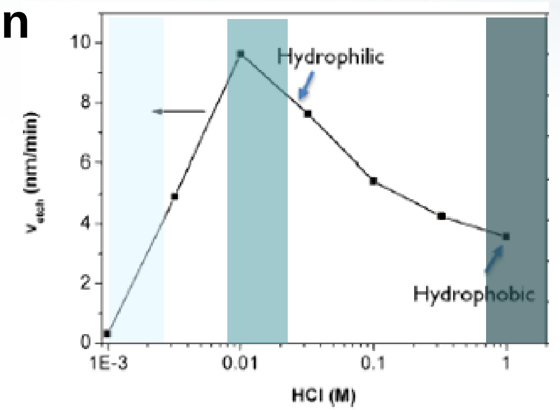


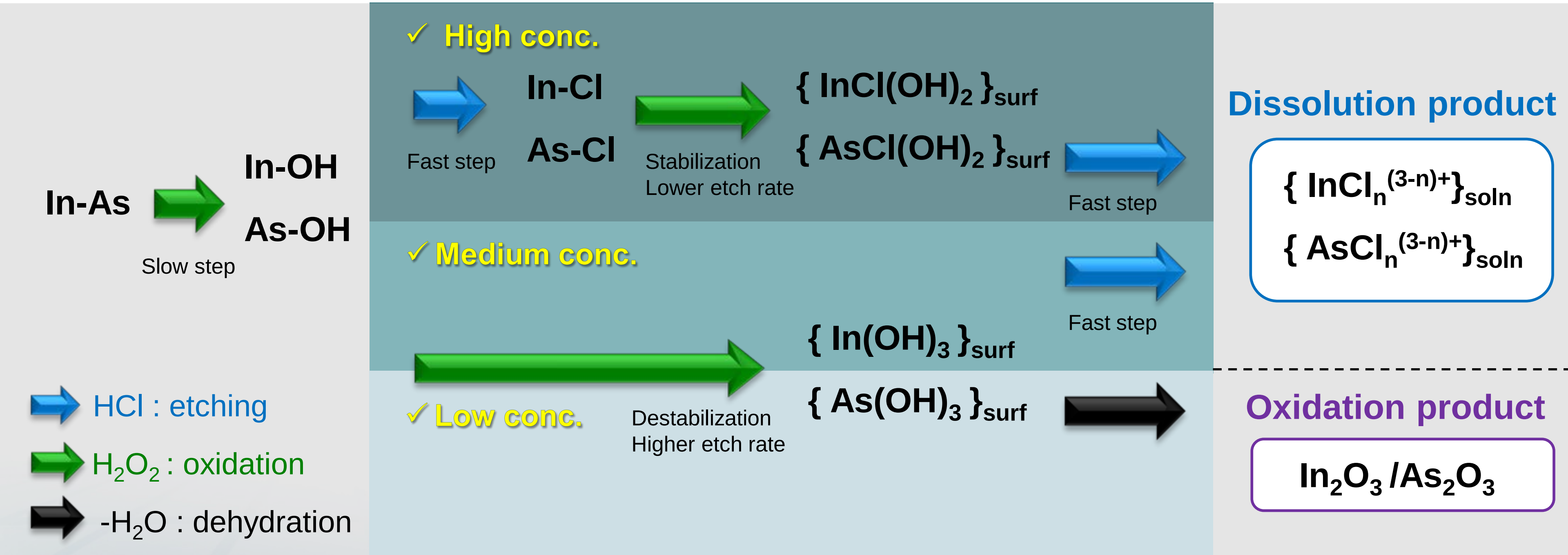


InAs Etching Mechanism of SC-2

❖ Etching mechanism according to the HCl concentration

- ✓ High concentration: oxidation rate **<** dissolution rate
- ✓ Low concentration : oxidation rate **>** dissolution rate





In-As → Slow step → **In-OH**, **As-OH**

✓ High conc.

→ Fast step → **In-Cl**, **As-Cl** → Stabilization, Lower etch rate → **$\{InCl(OH)_2\}_{surf}$**, **$\{AsCl(OH)_2\}_{surf}$** → Fast step

✓ Medium conc.

→ Fast step

✓ Low conc.

→ Destabilization, Higher etch rate → **$\{In(OH)_3\}_{surf}$**, **$\{As(OH)_3\}_{surf}$** →

Dissolution product

$\{InCl_n^{(3-n)+}\}_{soln}$

$\{AsCl_n^{(3-n)+}\}_{soln}$

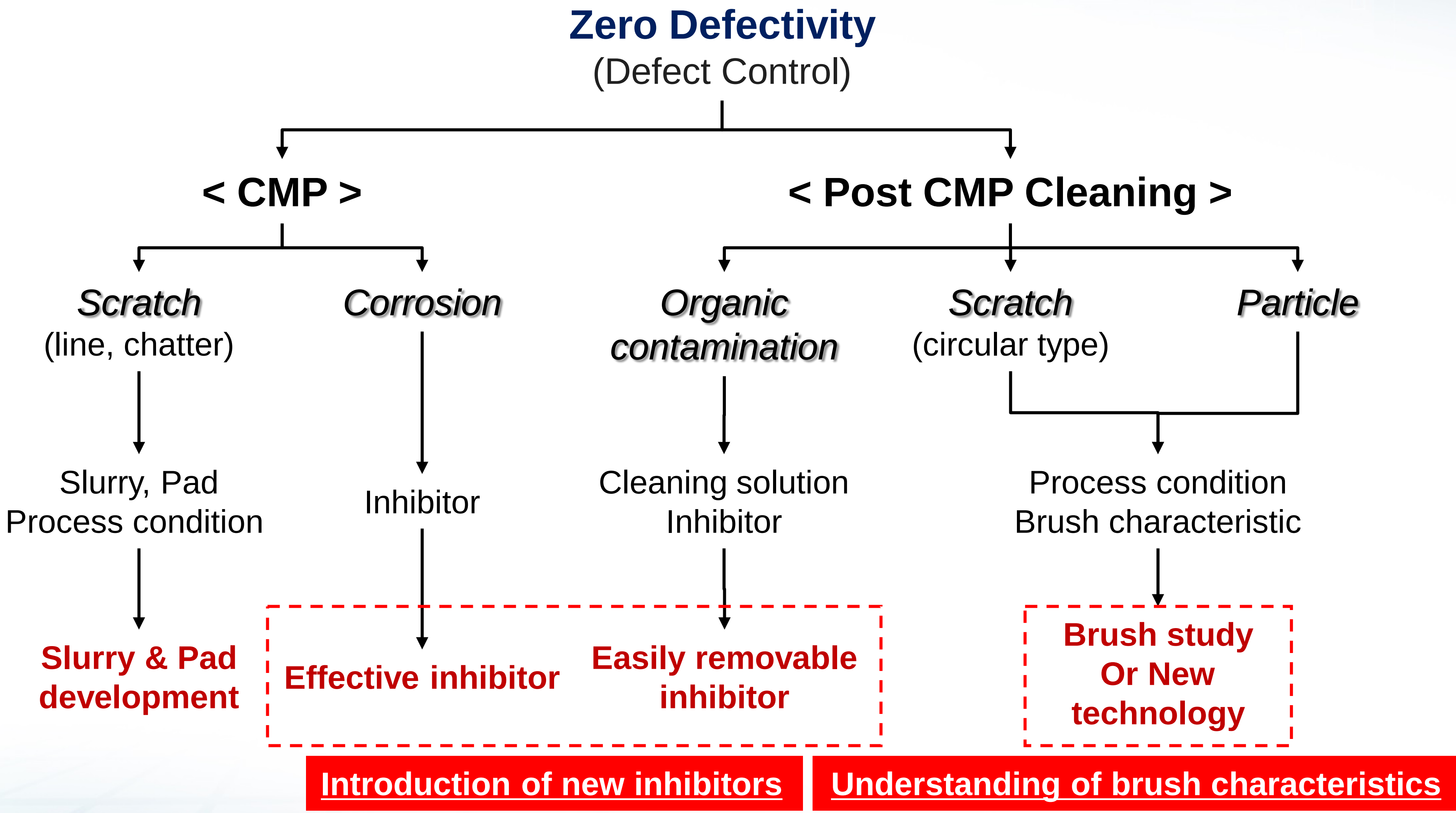
Oxidation product

In_2O_3 /As_2O_3

- 🟦 HCl : etching
- 🟩 H_2O_2 : oxidation
- ⬛ -H_2O : dehydration

Dennis H. Van Dorp, Sophia Arnauts, Frank Holsteyns and Stefan De Gendt, ECS Journal of Solid State Science and Technology, 4(6) N5061-N5066 (2015)

Defect Control Map



Zero Defectivity
(Defect Control)

< CMP >

Scratch
(line, chatter)
Slurry, Pad
Process condition
Slurry & Pad development

Corrosion
Inhibitor
Effective inhibitor

< Post CMP Cleaning >

Organic contamination
Cleaning solution
Inhibitor
Easily removable inhibitor

Scratch
(circular type)

Particle

Process condition
Brush characteristic
Brush study
Or New
technology

Introduction of new inhibitors

Understanding of brush characteristics

Synergy between cleaning system and chemistry

Summary

- CMP becomes more importance in 1x nm below device design and fabrication
- CMP Challenges : FEOL, MOL process- defect sensitive
- New consumable and cleaning technology needed
- Current cleaning process and technology are available and could solve all contamination issues in post CMP cleaning

THANK YOU