Chemical Mechanical Planarization

Stack Treck

Post CMP Cleaning Conference | Austin 2017 | Viorel Balan - CEA LETI

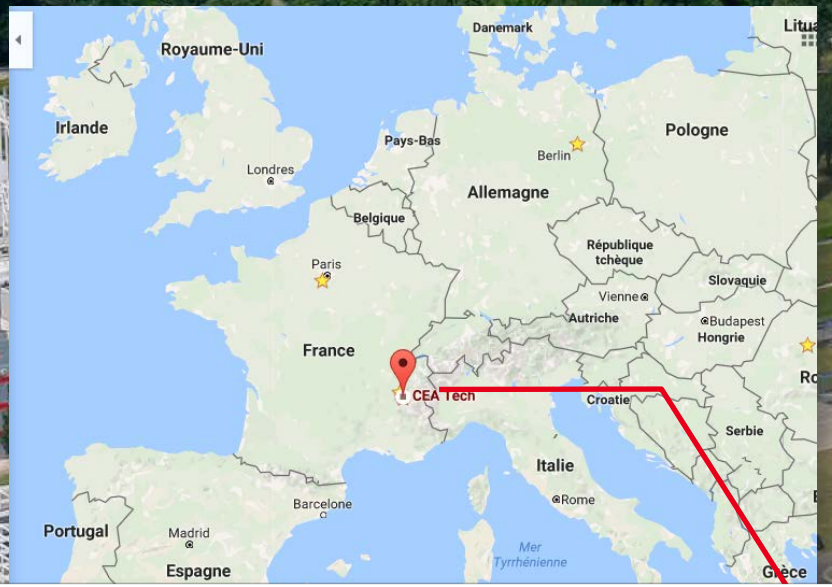
LETI AT THE GLANCE

Founded in 1967

318 M€ Budget
39 M€ Capex

1800 Collaborators
160 PhD + 40 post-doctorants
38 % foreign students

8500 m² clean room 24X7

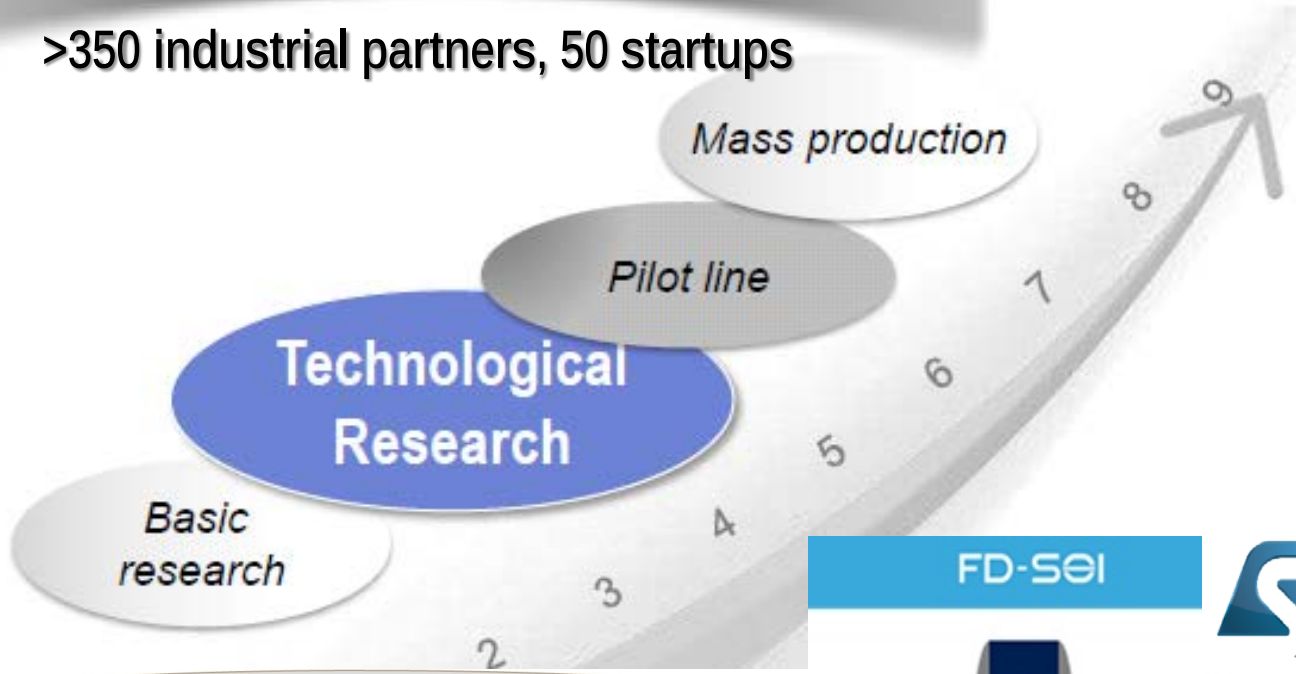


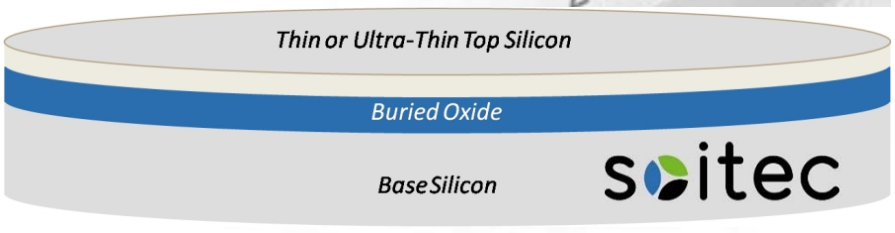
LETI

Mission

Create and transfer innovation to our industrial partners

>350 industrial partners, 50 startups





life.augmented

LETI

50 years

Create and transfer innovation to our industrial partners

- 50/ years of Pioneered Innovation @LETI (2017)
- 50/ years of Moore's Law (2015)

→ doubling the number of components on integrating circuit every year (or two..)

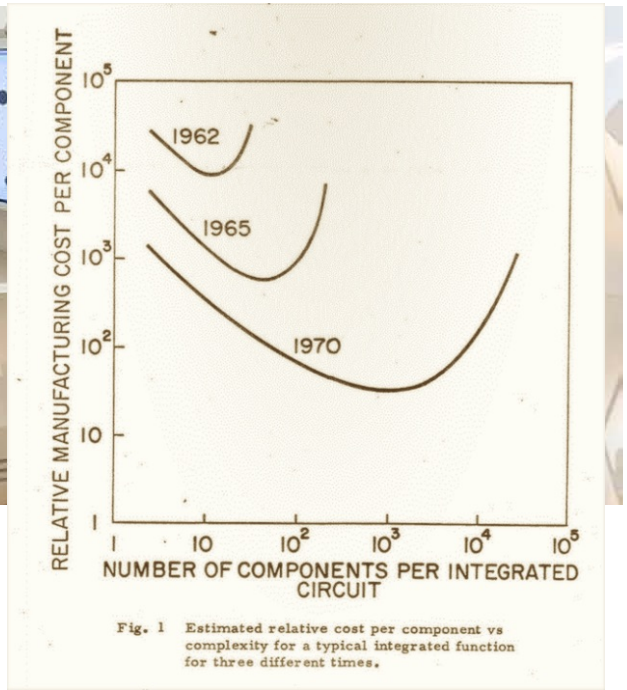


Fig. 1 Estimated relative cost per component vs complexity for a typical integrated function for three different times.

Moore's Law

50 years

Create and transfer innovation to our industrial partners

- 50/ years of Pioneered Innovation @LETI (2017)
- 50/ years of Moore's Law (2015)

→ doubling the number of components on integrating circuit every 18 months

↗ Scaling Up: ↗ Chip Area → Moore 1.0

↘ Scaling Down: ↘ Size&Cost/Transistor → Moore 2.0

Chris Mack, Multiple Lives of Moore's Law

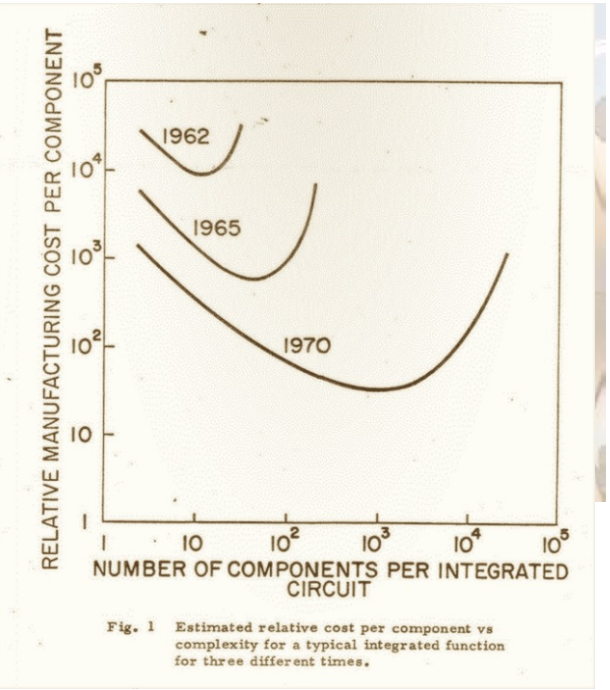


Fig. 1 Estimated relative cost per component vs complexity for a typical integrated function for three different times.

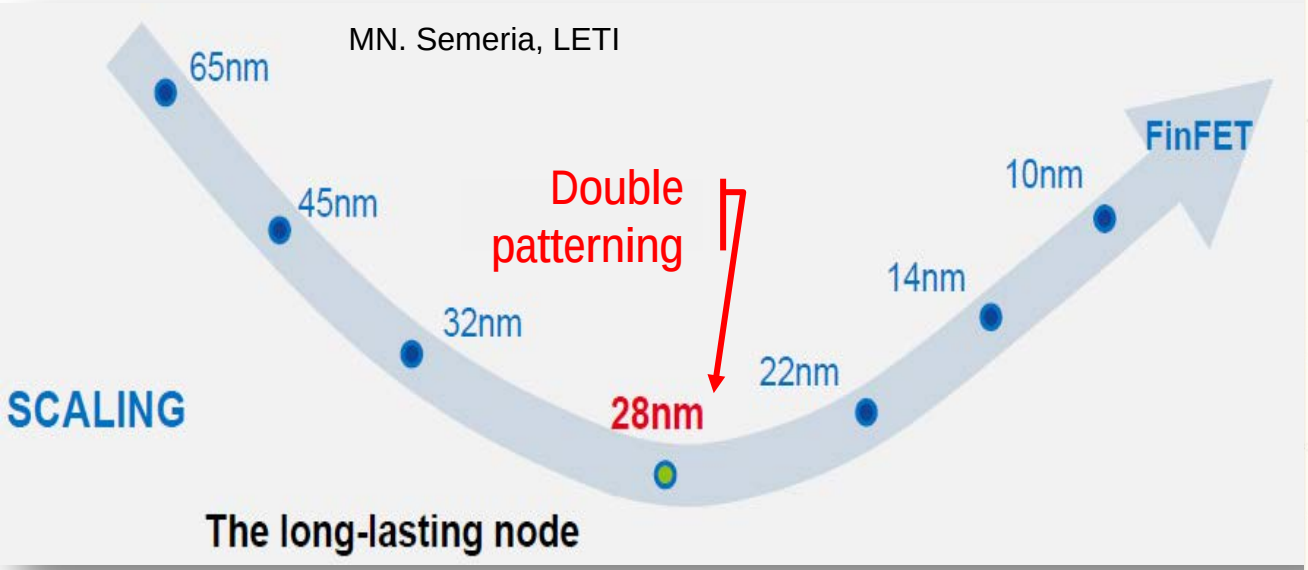
Moore's Law

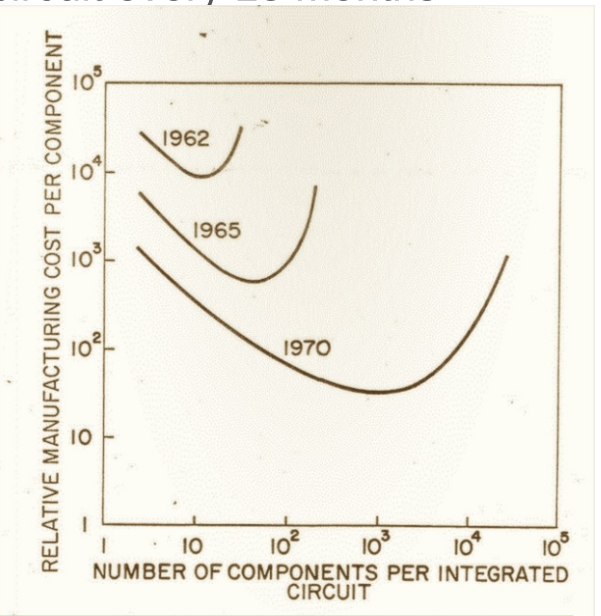
50 years

Create and transfer innovation to our industrial partners

- 50/ years of Pioneered Innovation @LETI (2017)
- 50/ years of Moore's Law (2015)

→ doubling the number of components on integrating circuit every 18 months





Cost /Transistor Increase below 28nm→ Lithography Double Patterning

The Law is Dead

Long Live The Law

Create and transfer innovation to our industrial partners

- 50/ years of Pioneered Innovation @LETI (2017)
- 50/ years of Moore's Law (2015)

→ doubling the number of components on integrating circuit every 18 months

- ↗ Scaling Up: ↗ Chip Area → Moore 1.0
- ↘ Scaling Down: Size&Cost/Transistor → Moore 2.0
- ↗ « Device Cleverness » → Moore 3.0

Chris Mack, Multiple Lives of Moore's Law

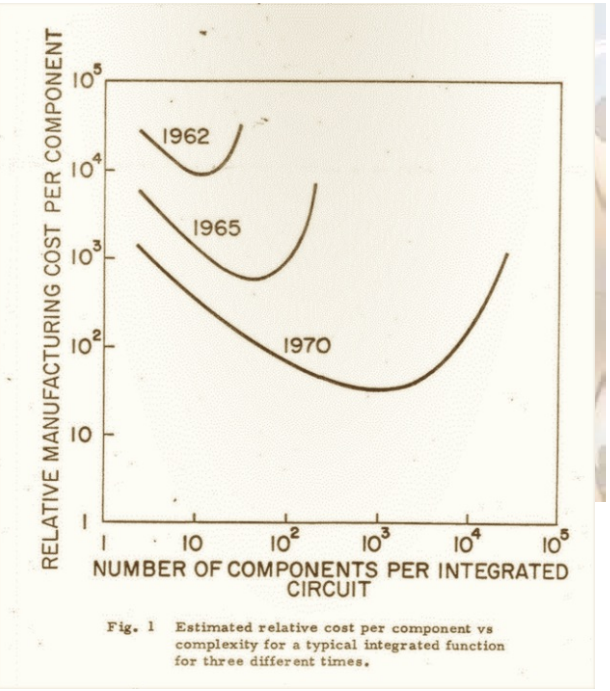
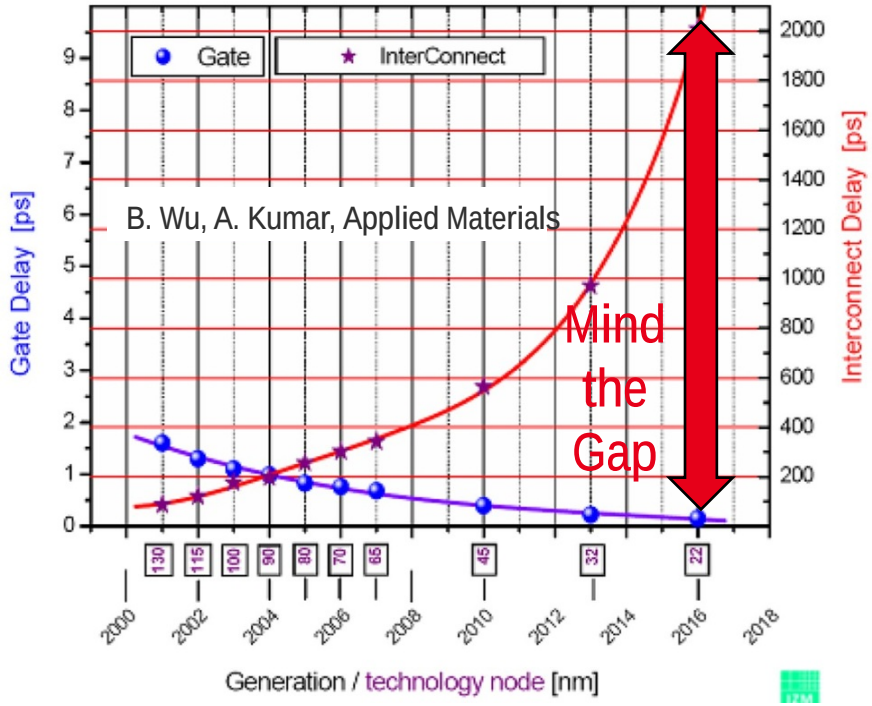


Fig. 1 Estimated relative cost per component vs complexity for a typical integrated function for three different times.

Moore's Law ~~2~~→3.0

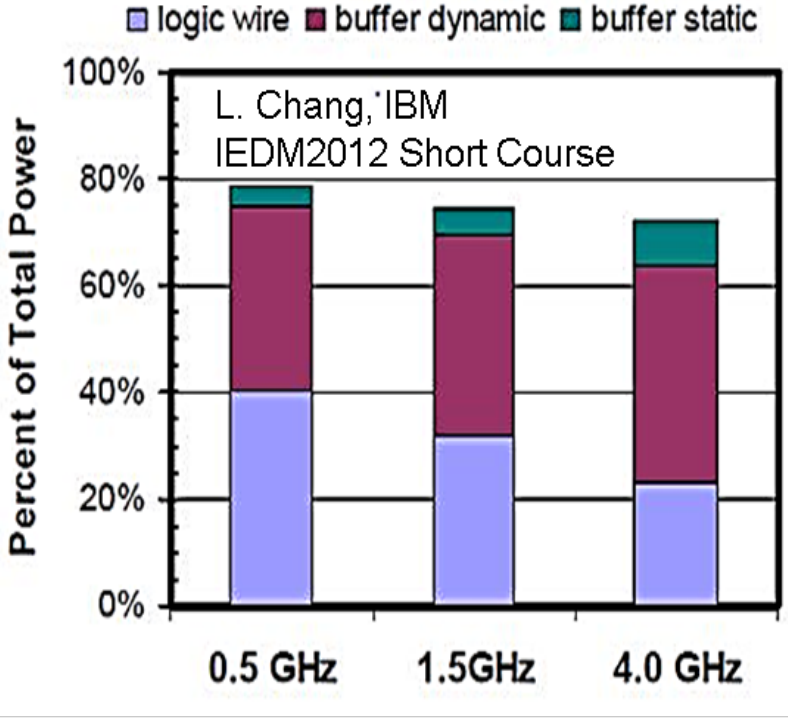
~~Scale to Go Down~~ → Stack to Go Up → 3D Integration

Gate & Interconnect Delay



Growing Gap Gate-Wire Performances

Total Power



80% Power consumed by Interconnects

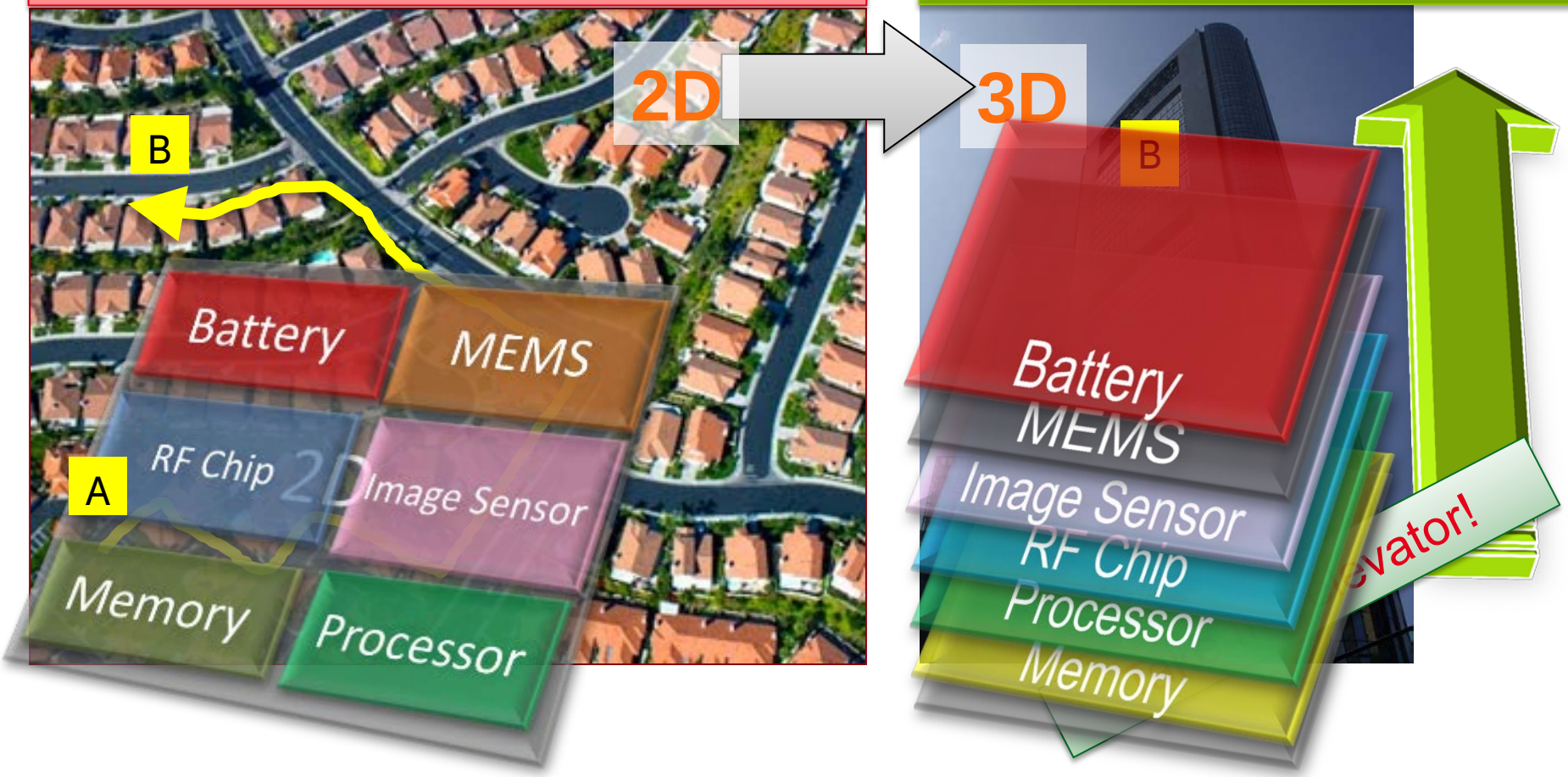
« Need Proper Consideration of Wires » ↘ Distances

Stacking Heterogenous Devices

Device Cleverness

Delay? Power?

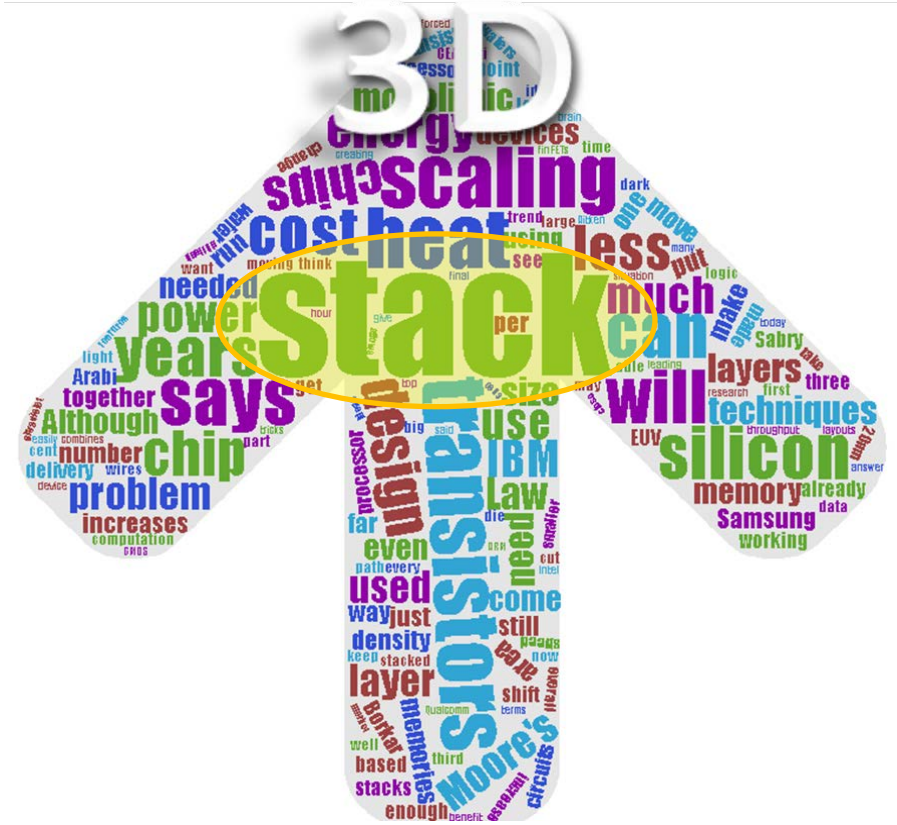
Exploit the3rd dimension



Stacking Heterogenous Devices: ↘ (Delay, Power, Size) ↗ Cleverness

Red Is The New Blue

Stacking Is The New Scaling



Lithography Enables Scaling / CMP Enables Stacking

Building Stacked Devices by Hybrid Direct Bonding

Challenges

Direct Bonding → Roughness & Clean SiO_2 & Cu Non-Patterned Wafers

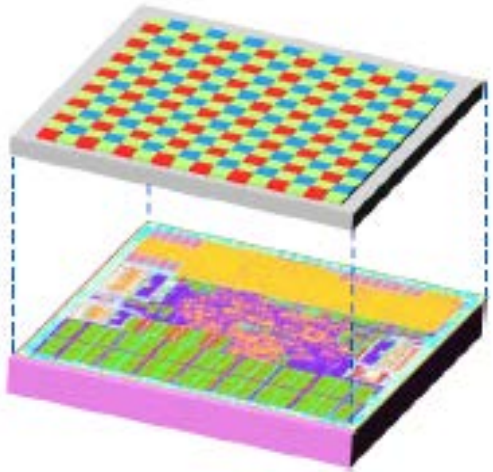
Hybrid Direct Bonding → Patterned Wafers Topography: Local/Global

Conclusion

Stacking Heterogenous Devices

Application to 3D Stacked Back Side Imagers

3D stacked BSI Imager



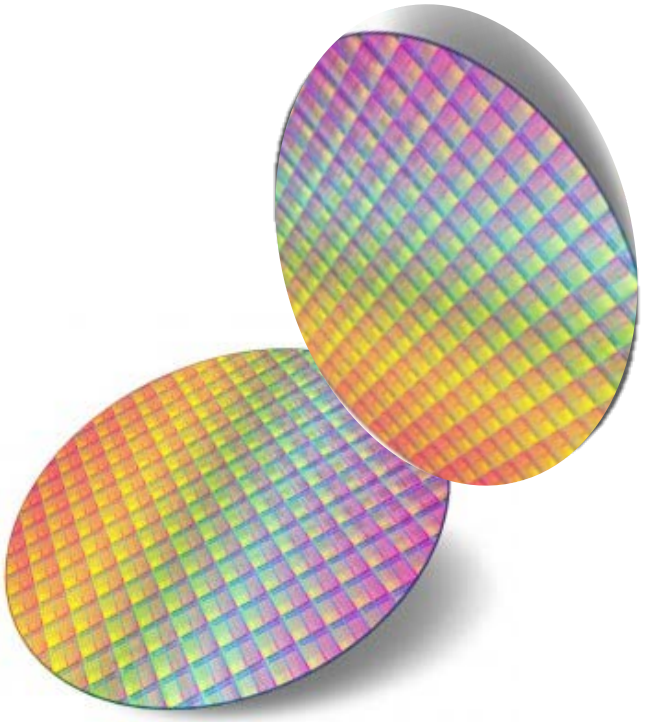
J. Chossat 3D Summit Grenoble 2016

Top die

- Pixels

Bottom die

- Analog & Readout
- Sensor Logic
- And more !!!



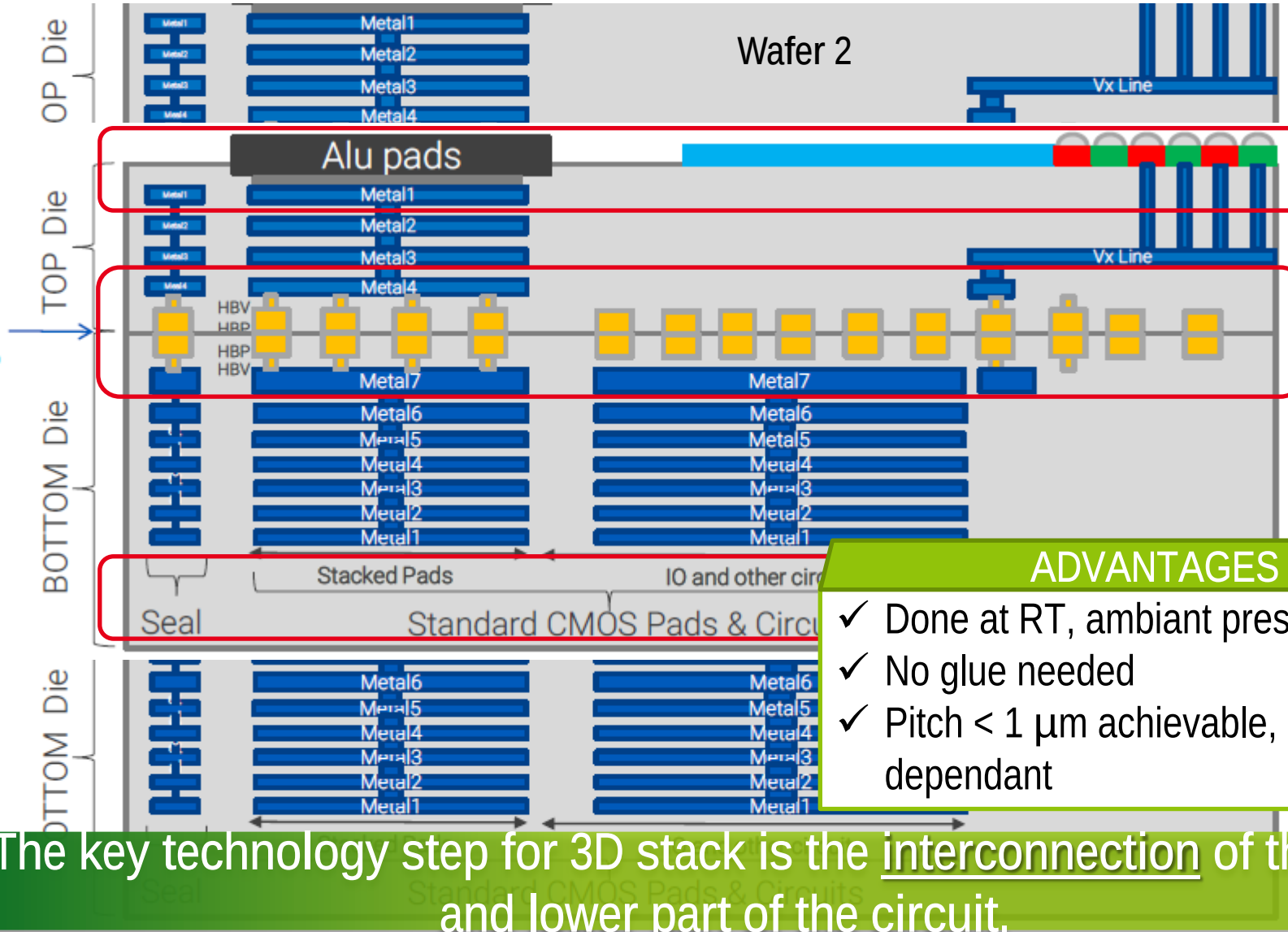
- Wafer to Wafer Stacking by Hybrid Direct Bonding Technology
  - → Top Die Contains only Pixels
  - → Passive Substrate replaced by Advanced Digital CMOS wafer

Manufacturing Flexibility →
Different Technology Nodes (Design Rules) for different components

Stacking Heterogenous Devices

3D Stacked BSI by Hybrid Direct Bonding

J. Chossat 3D Summit Grenoble 2016



ADVANTAGES

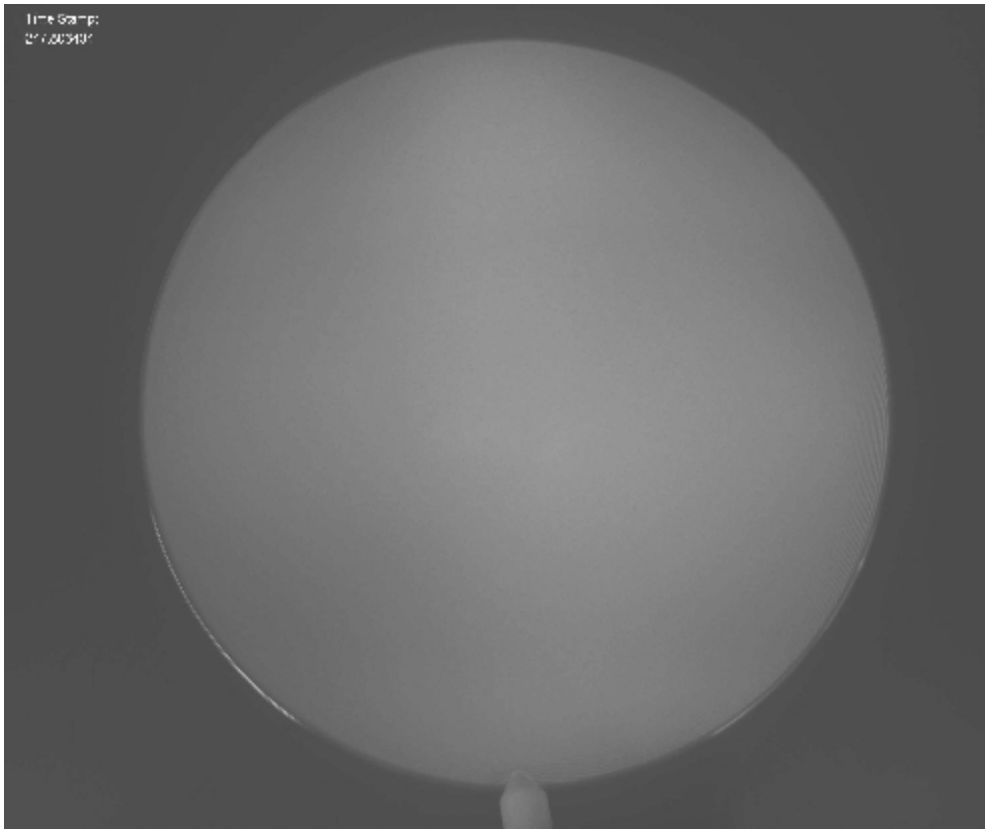
- ✓ Done at RT, ambiant pressure
- ✓ No glue needed
- ✓ Pitch < 1 µm achievable, alignment dependant

The key technology step for 3D stack is the interconnection of the upper and lower part of the circuit.

Direct Bonding

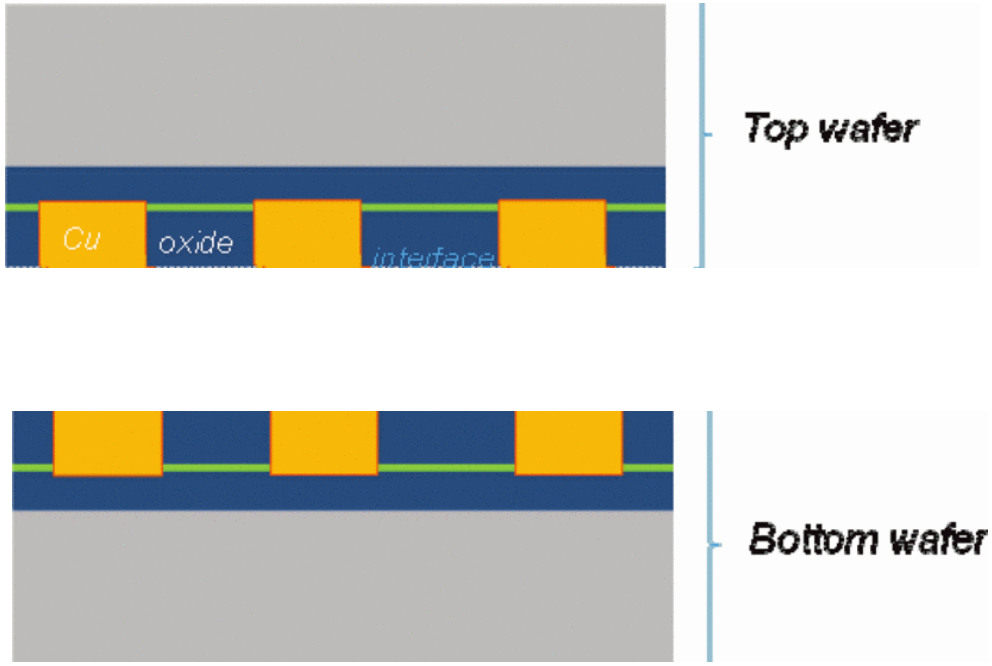
Definition

Process by which two sufficiently **flat** and **clean** surfaces can spontaneously bond to each other without any added adhesive layer, at room temperature



Allows different materials to be stacked together w/o concern for the crystalline relationship to one another →SOI wafers (silicon-on-insulators) or innovative engineered substrates.

From Direct Bonding
To Hybrid Direct Bonding



Dielectric
Mechanical Strength
SiO_2

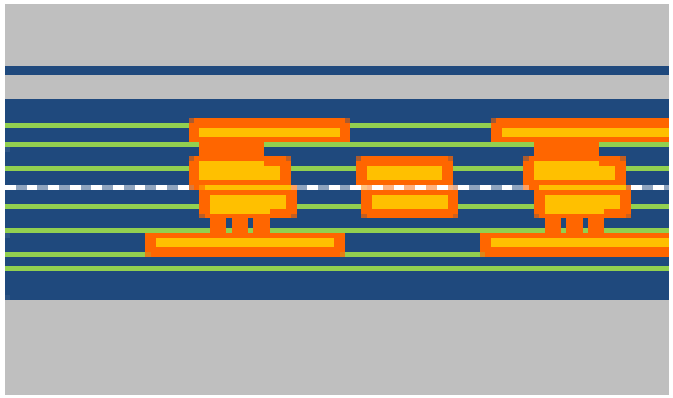
+

Metal
Electrical connection
Cu: microelectronic

- Cu → most promising 3D integration candidate
  - Main metal used for CMOS interconnects
  - Cost of ownership
- Copper/oxide surface direct bonding advantages:
  - Very high interconnect density possible.
  - Low-temperature process
  - Compatibility FEOL/BEOL requirements for a sequential approach

Chemical Mechanical Planarization

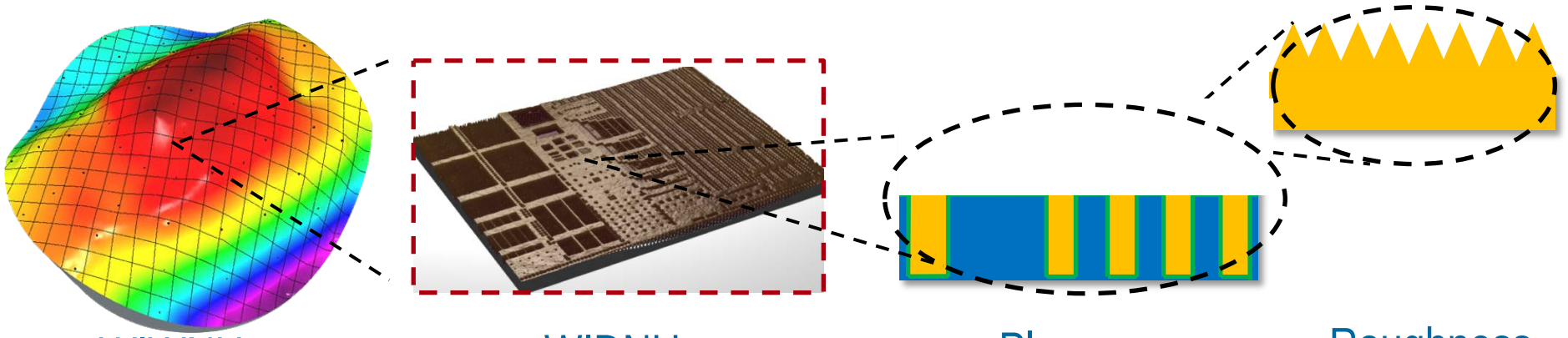
Challenges for Recreating The Bulk from 2 Mixt Surfaces



Bond 2 Surfaces with

- Cu
- Barrier
- Dielectric

→ Manage Topography

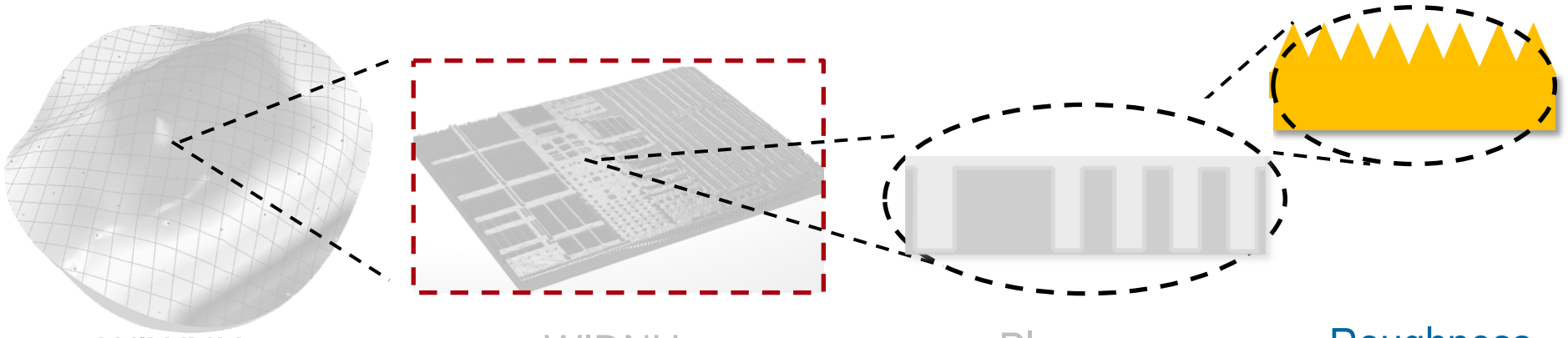


WIWNU	WIDNU	Planar	Roughness
Diameter Planar	*Die Planar*	*Device Planar*	*Atomic Planar*

Intimate Surface Contact Needed → Planarization @all Spatial λ

Chemical Mechanical Planarization

Challenges for Recreating The Bulk from 2 Surfaces



WIWNU

Diameter Planar

WIDNU

Die Planar

Planar

Device Planar

Roughness

Atomic Planar

Direct Bonding SiO_2

Roughness Impact

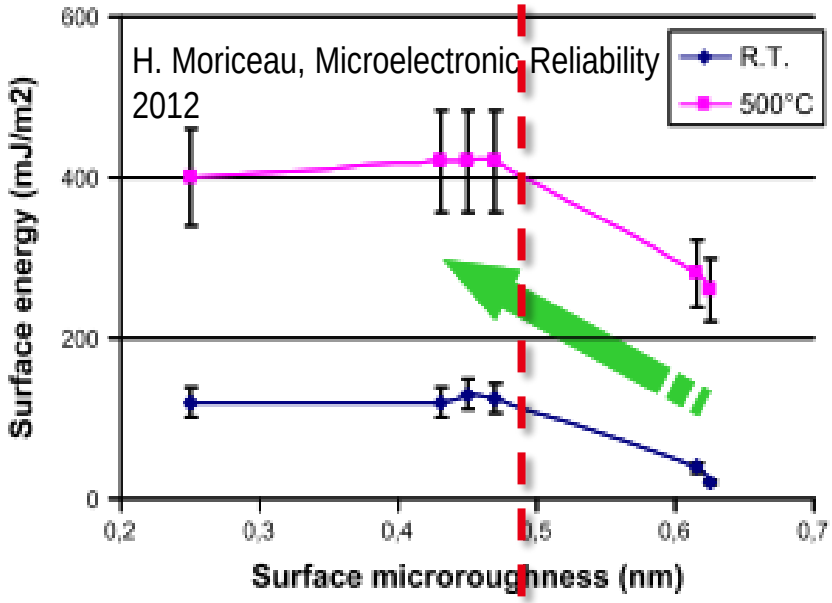
F. Rieutord, ECS 2006

Atomic bonding

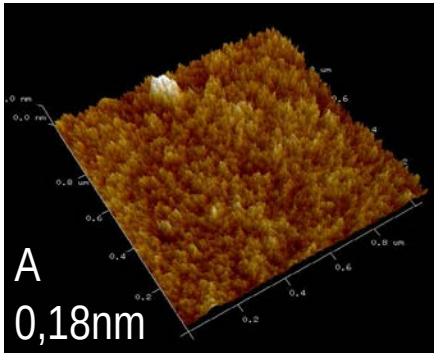
- *Van der Waals force*
- *Covalent bonds*
- *Metallic bonds*

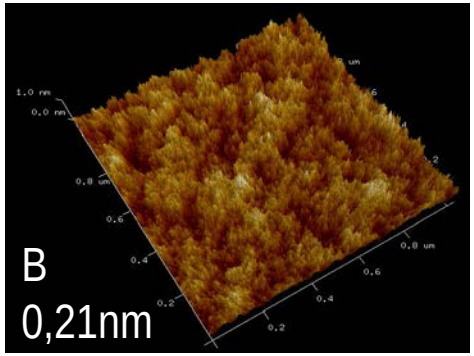
Annealing

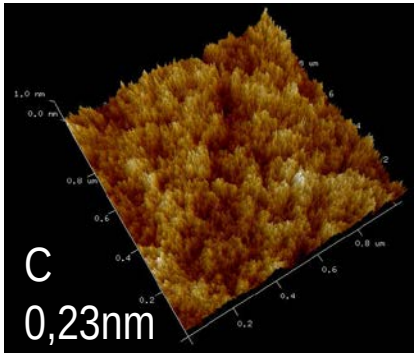
Complete sealing

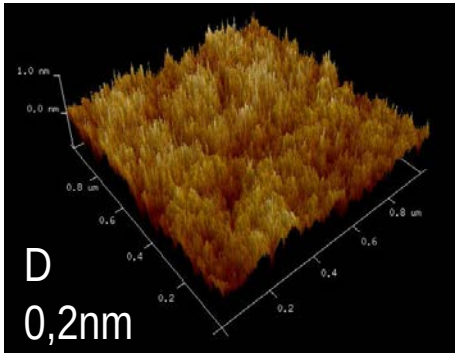


Surface high frequency micro-roughness → key role in the bonding phenomenon,
Low frequency roughness can be accommodated by deformation of each substrate (elastic energy price)







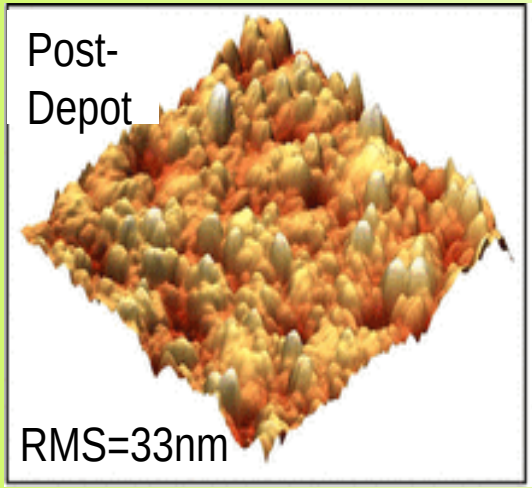


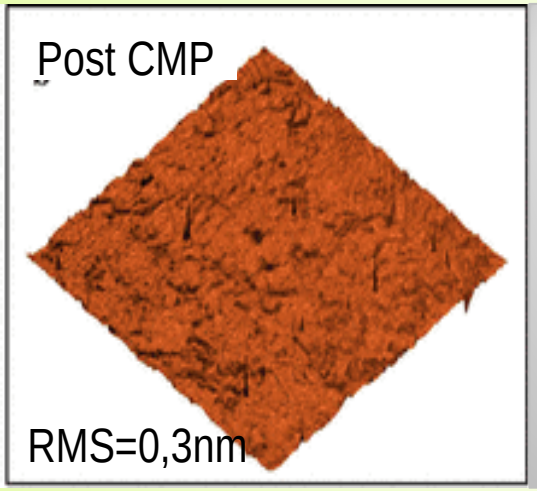
SiO_2/SiO_2 Blanket Bonding RMS<0.5nm

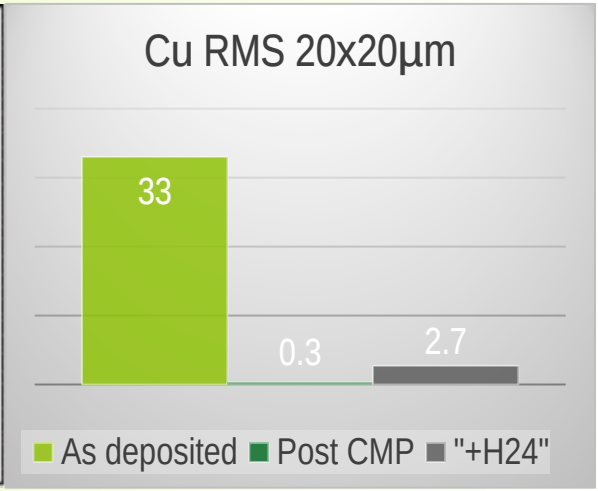
Direct Bonding

Cu-Cu

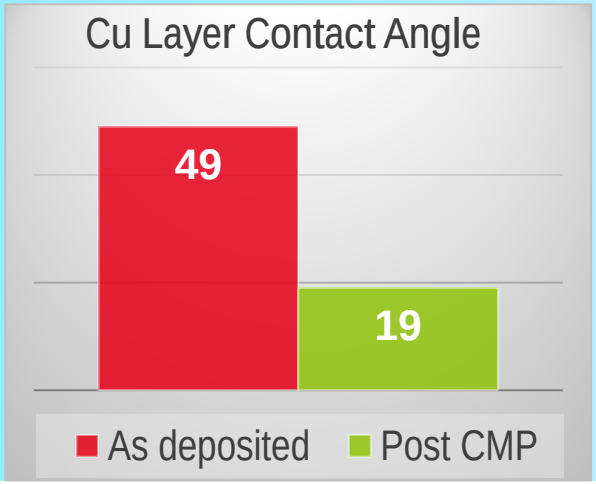
Roughness

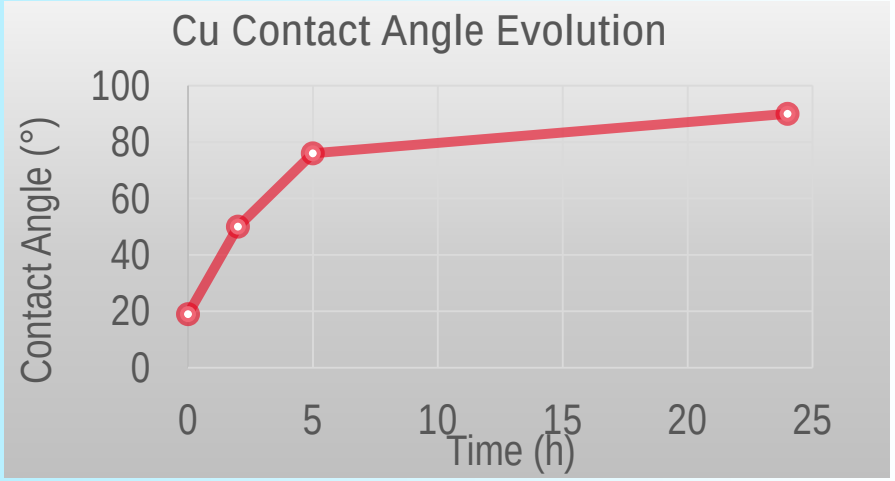






Hydrophilicity



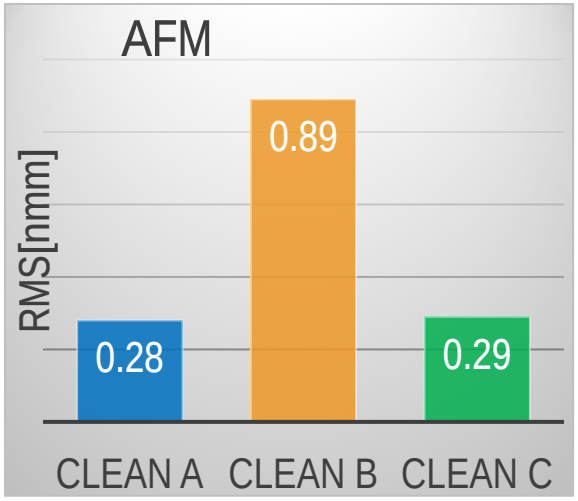


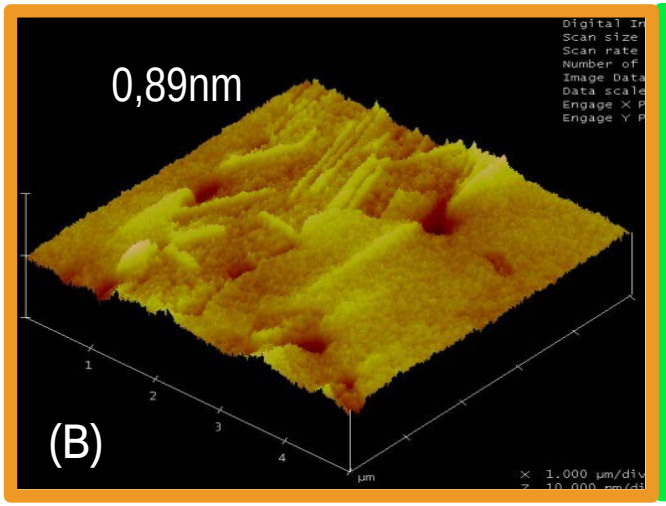
P. Gueguen ECS 2008

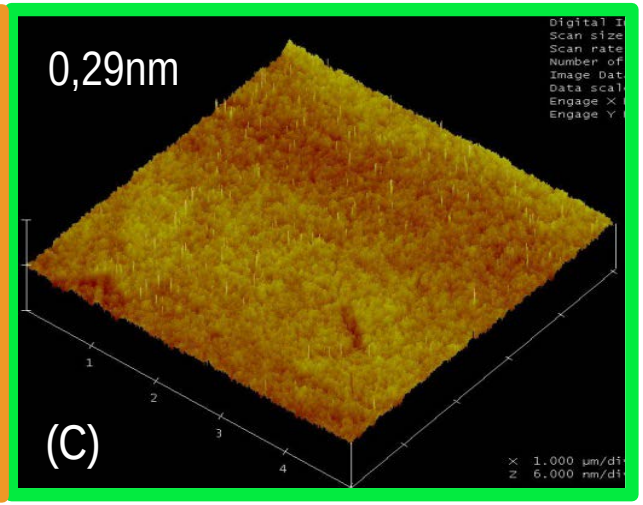
RMS & Contact Angle Increase → Q Time Impact

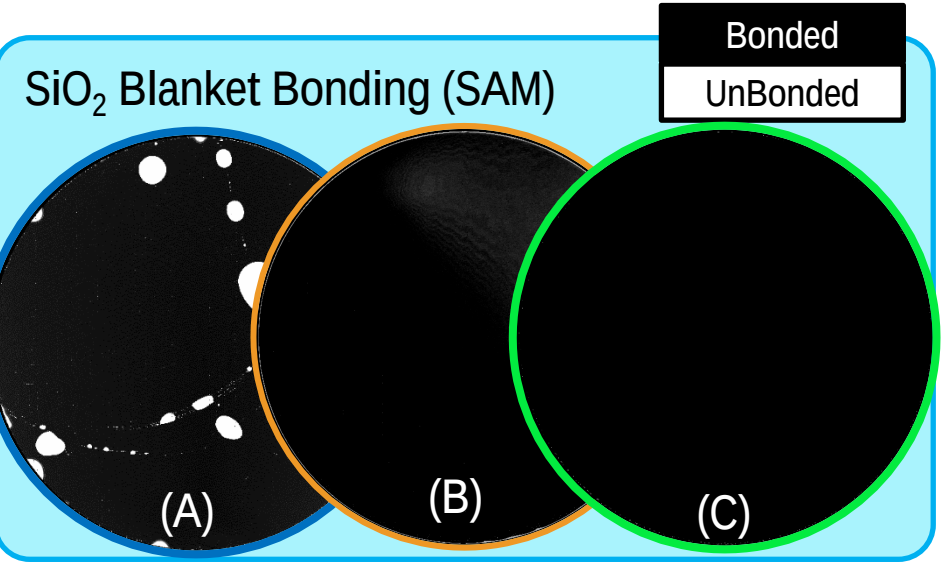
Direct Bonding

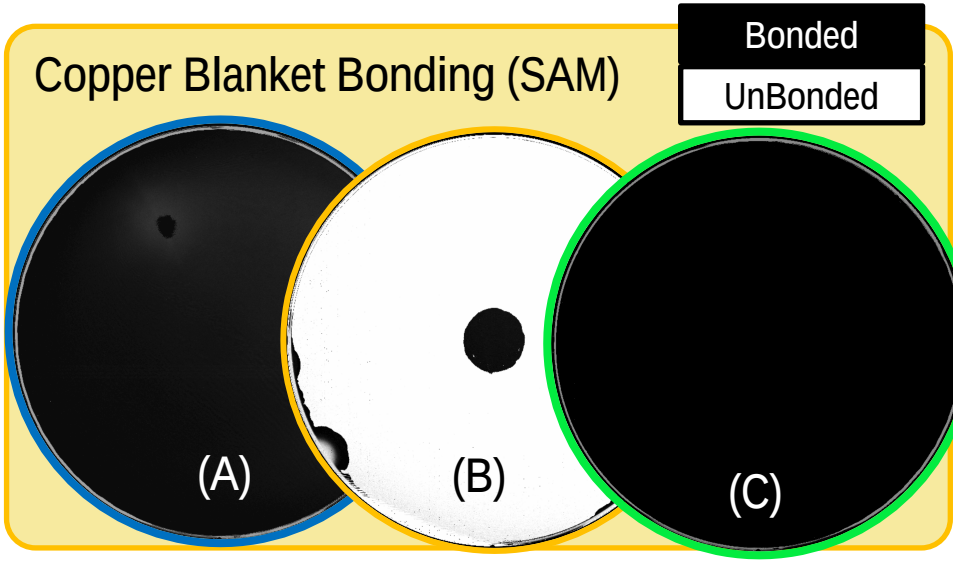
Cleaning Influence











Cleaning Solution Adapted both to Cu & SiO_2

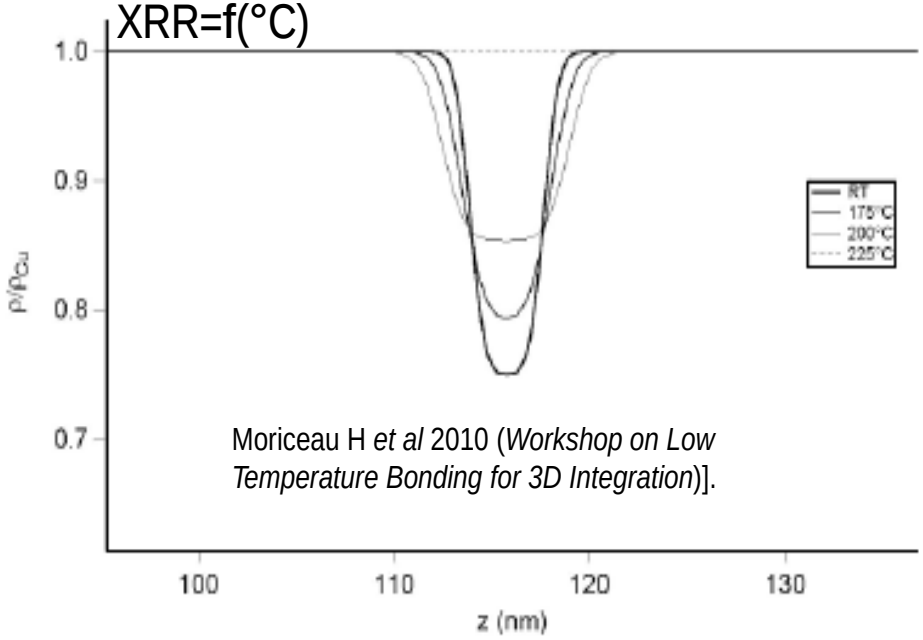
Direct Bonding

Cu-Cu Interface Evolution=f(T°C)

Cu-Cu Interface=f(°C) by TEM

- Thin copper oxide interfacial layer at the bonding interface
- 200°C, this copper oxide becomes thermodynamically unstable → grain growth→ sealing: XRR
- Bonding interface turns into a grain boundary with a high bonding energy

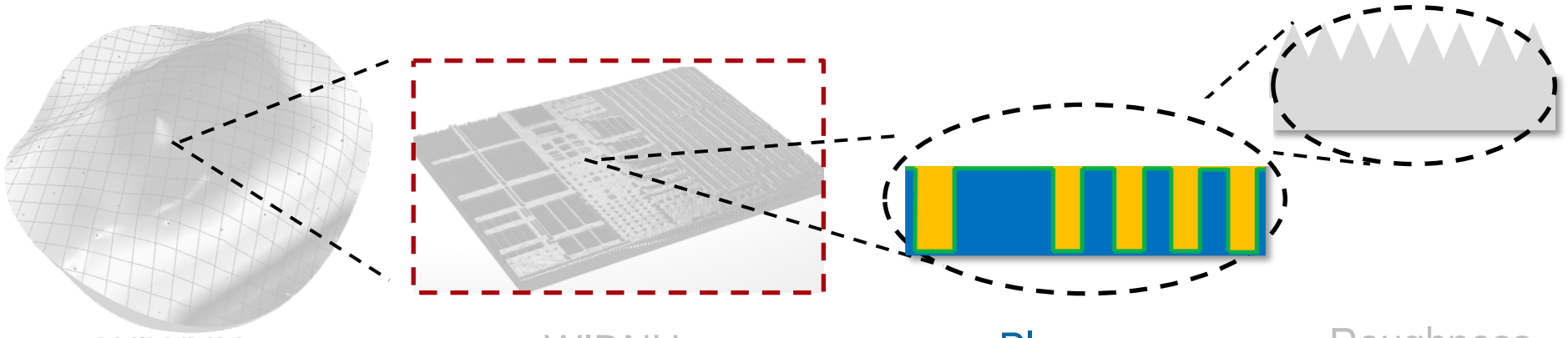
XRR=f(°C)



Moriceau H *et al* 2010 (*Workshop on Low Temperature Bonding for 3D Integration*)].

Chemical Mechanical Planarization

Challenges for Recreating The Bulk from 2 Surfaces



WIWNU

Diameter Planar

WIDNU

Die Planar

Planar

Device Planar

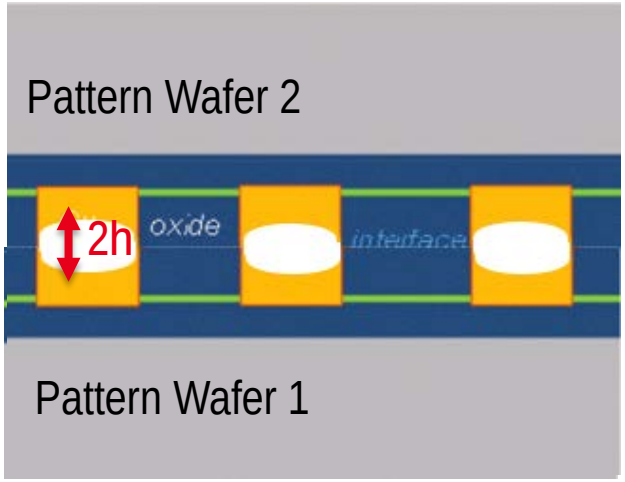
Roughness

Atomic Planar

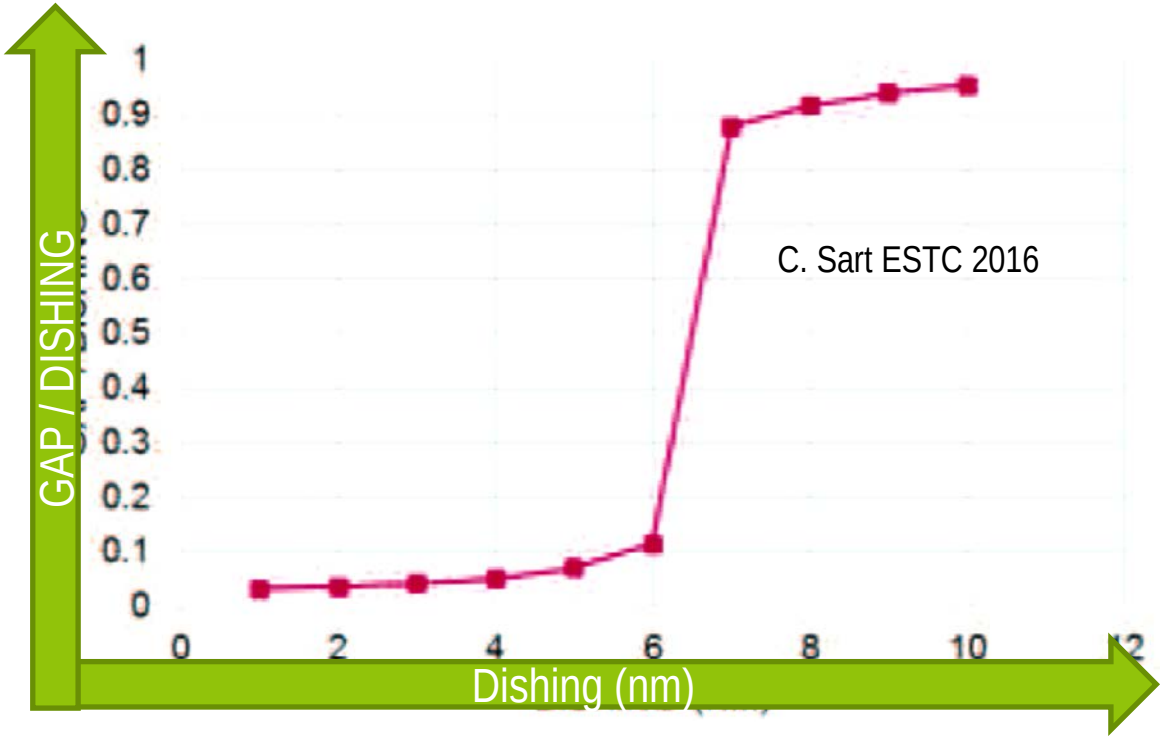
Hybrid Direct Bonding

Local Topography Impact Modelisation

- Dishing critical: topography doubled → negative impact electrical contact



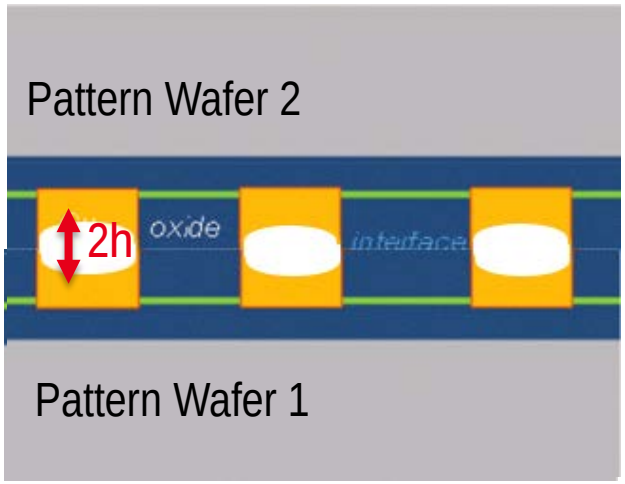
- Cohesive tractions effective below threshold value



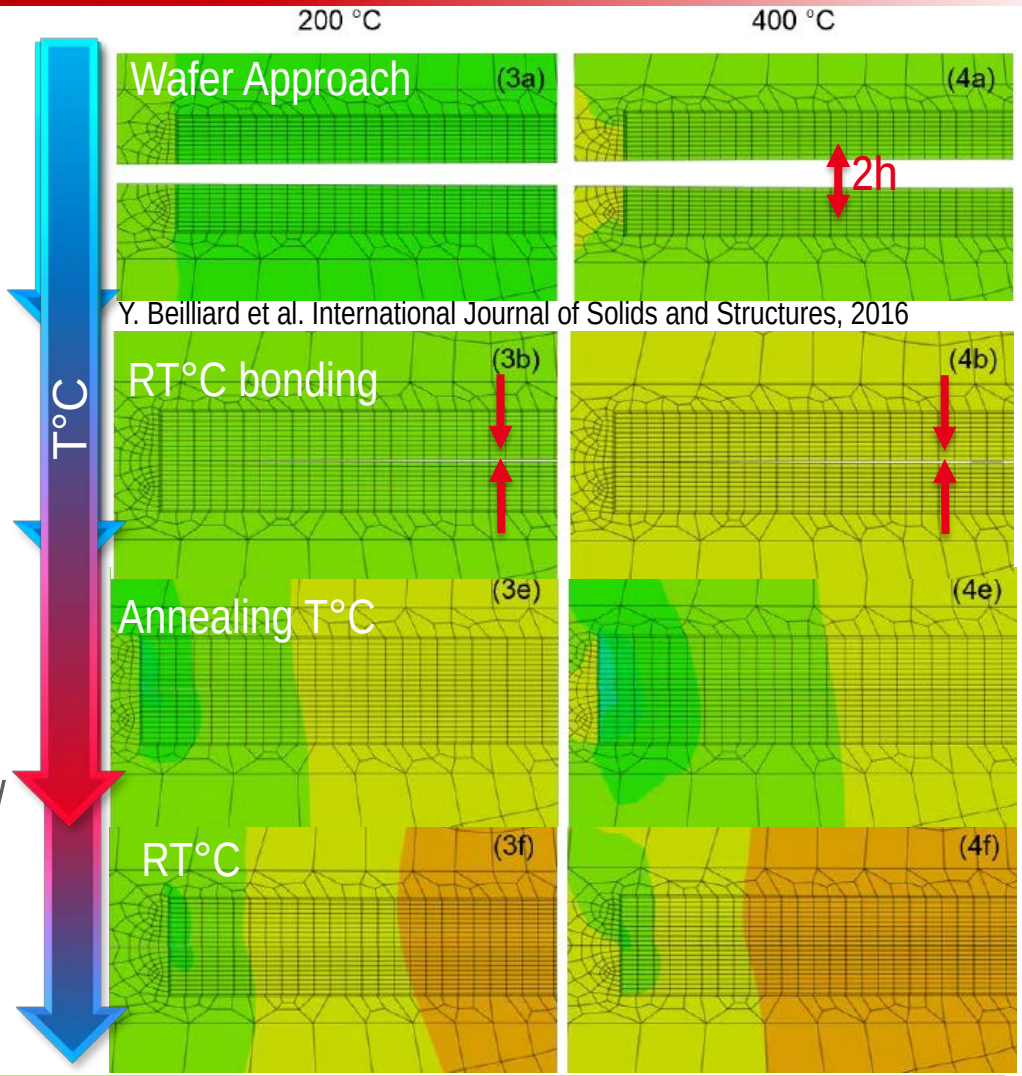
Hybrid Direct Bonding

Local Topography Impact Modelisation

- Dishing critical: topography doubled → negative impact electrical contact



- Small dishing of Cu pads overcome during post bond annealing even @ low T°C: 200°C

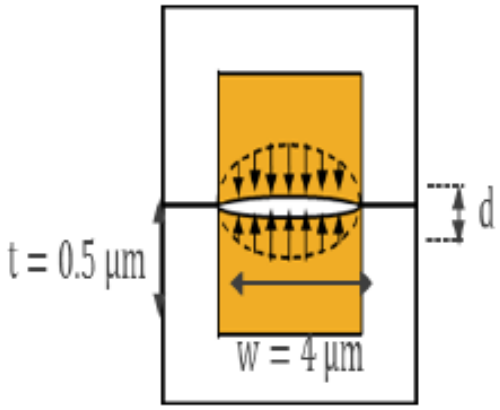


Cu/Cu Interface Remains Closed after Cooling Down to Room Temperature
Agreement w/ Experimental Results

Hybrid Direct Bonding

Predictive Model

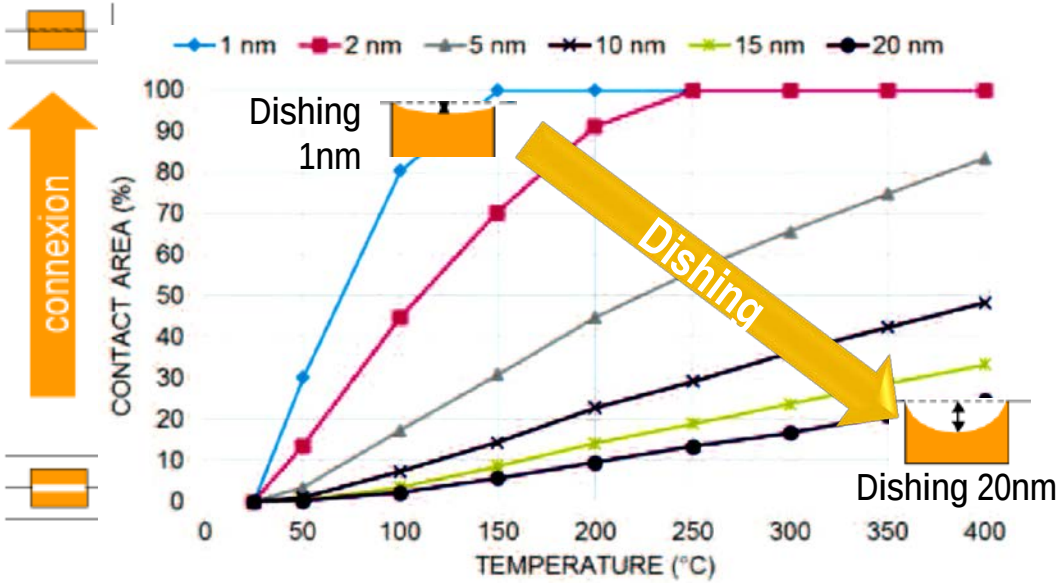
Model



In case of initial dishing in Cu pads

► Definition of the gap after thermal budget

Thermal budget post bonding



Forecast on % pad closure depending on anneal temperature

- Clues for process adaptation with dishing,
- Further models with introduction of grain size and crystal orientation.

S. Lhostis European 3D Summit 2017

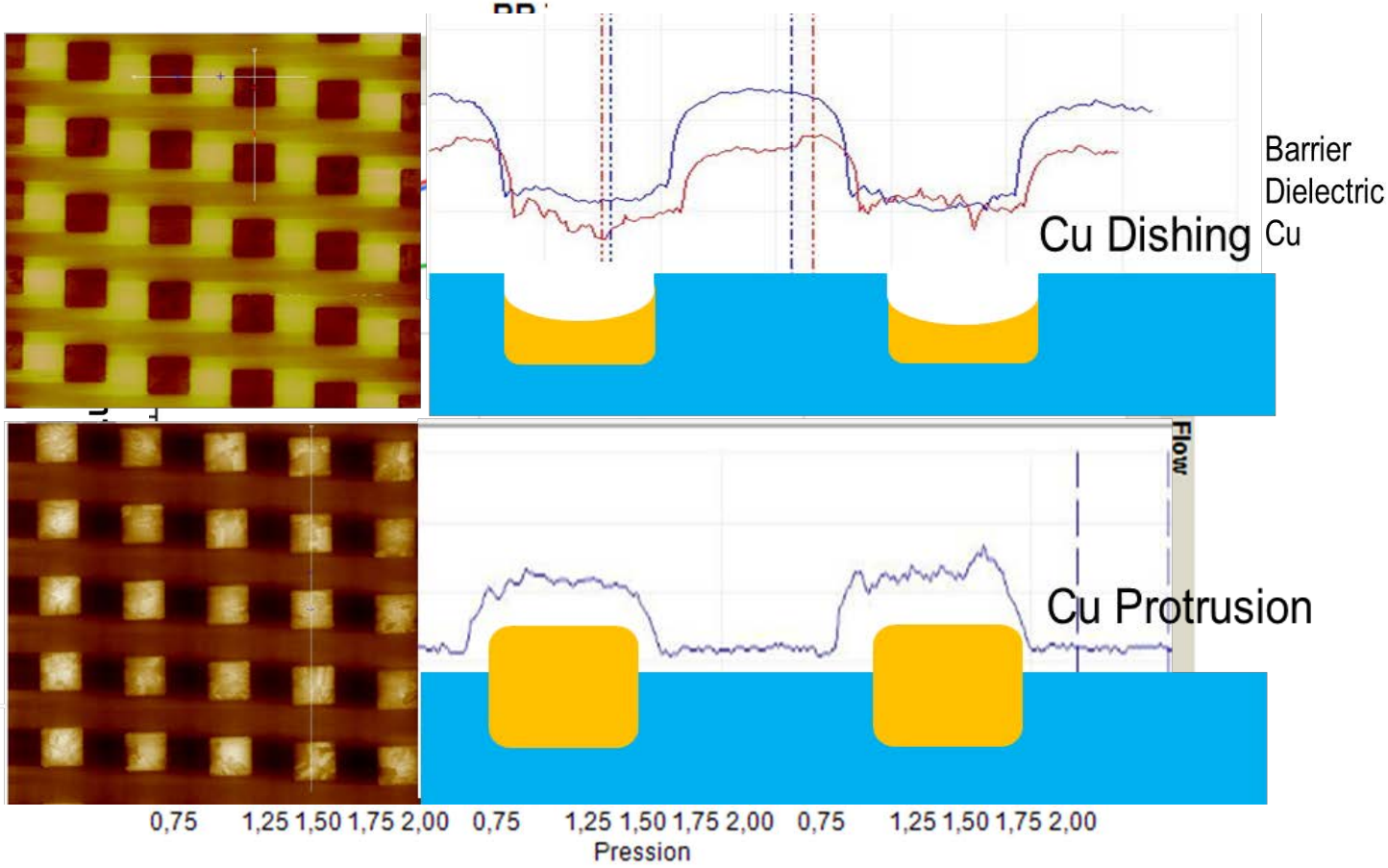
C. Sart ESTC 2016

Predictive Model for the Process of Hybrid Bonding Layer

Hybrid Direct Bonding

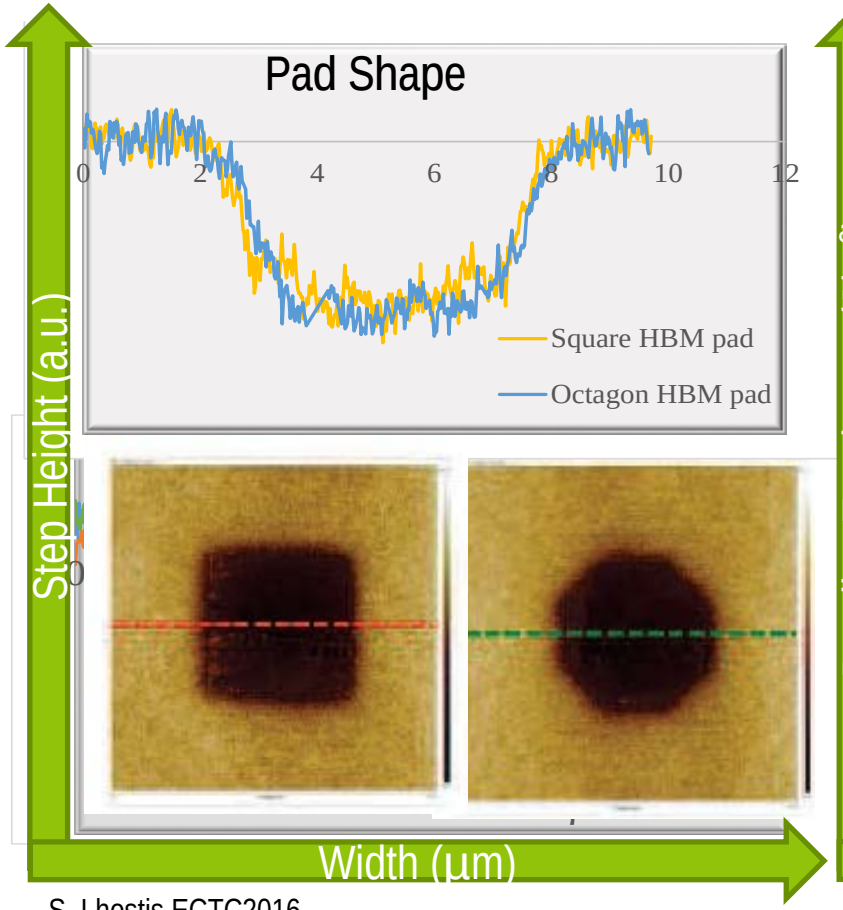
Patterned Wafers DOE

- >250 process conditions used → pads, slurries, %abrasif %/oxydant, V,P, flow, time…

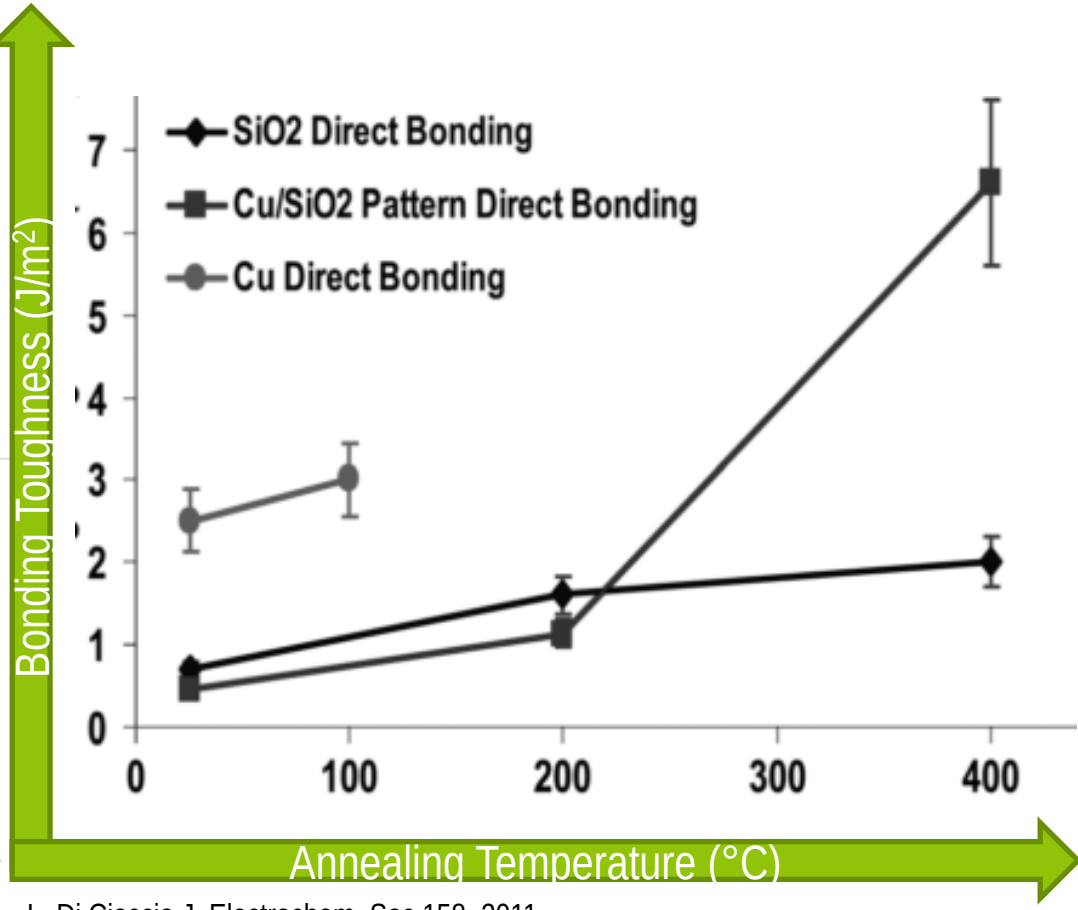


Hybrid Direct Bonding

Process Optimization



S. Lhostis ECTC2016

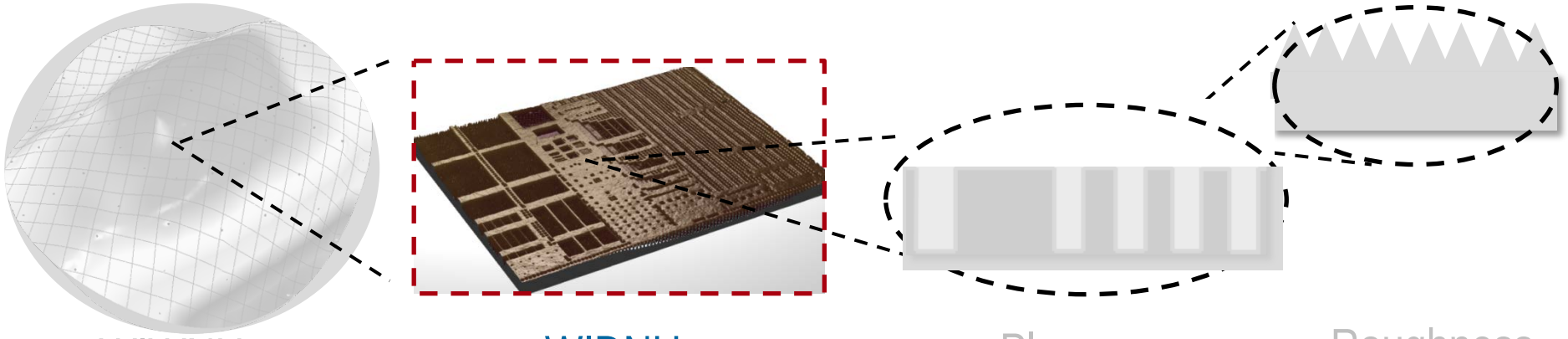


L. Di Cioccio J. Electrochem. Soc,158, 2011

Very Low Dishing, Uniform vs Cu Pad Shapes & Sizes
High Bonding Toughness Obtained

Chemical Mechanical Planarization

Challenges for Recreating The Bulk from 2 Surfaces



WIWNU

Diameter Planar

WIDNU

Die Planar

Planar

Device Planar

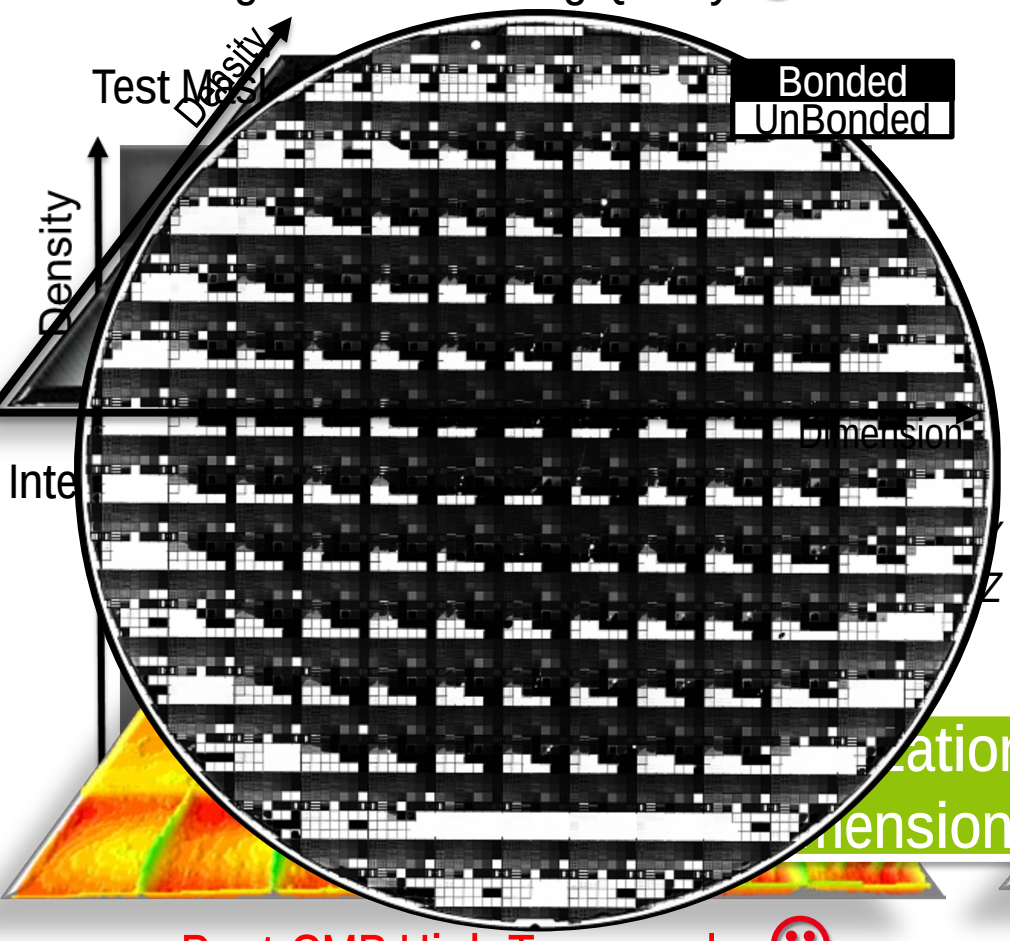
Roughness

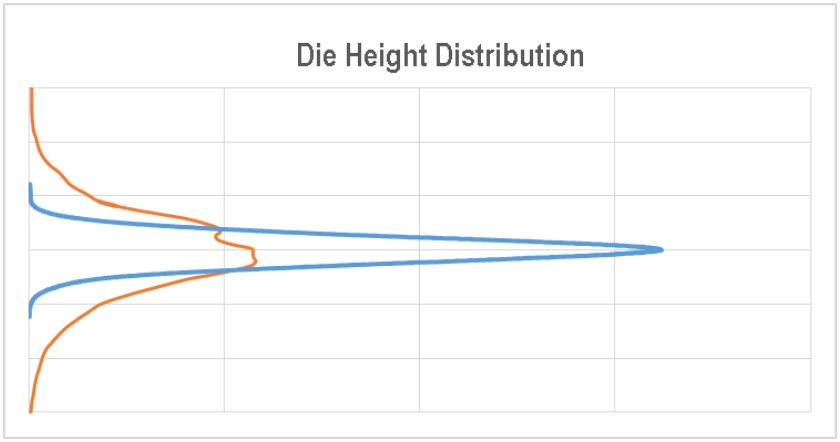
Atomic Planar

Stacking Heterogenous Devices

Dimension & Density Impact

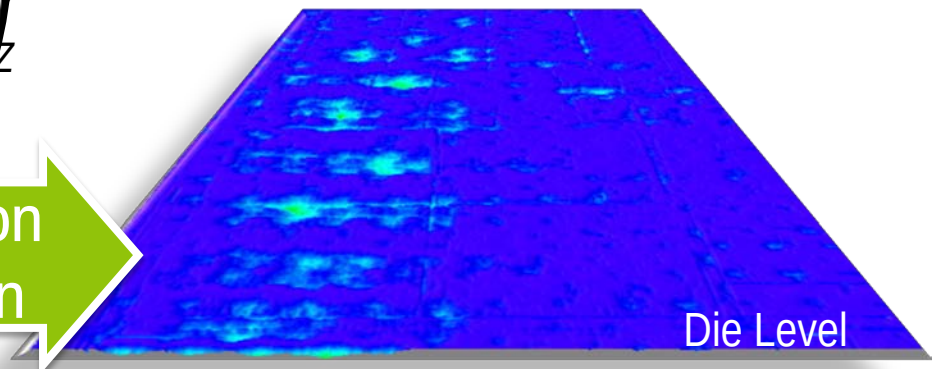
SAM Image→ Low Bonding Quality ☹





Post-CMP High Topography ☹

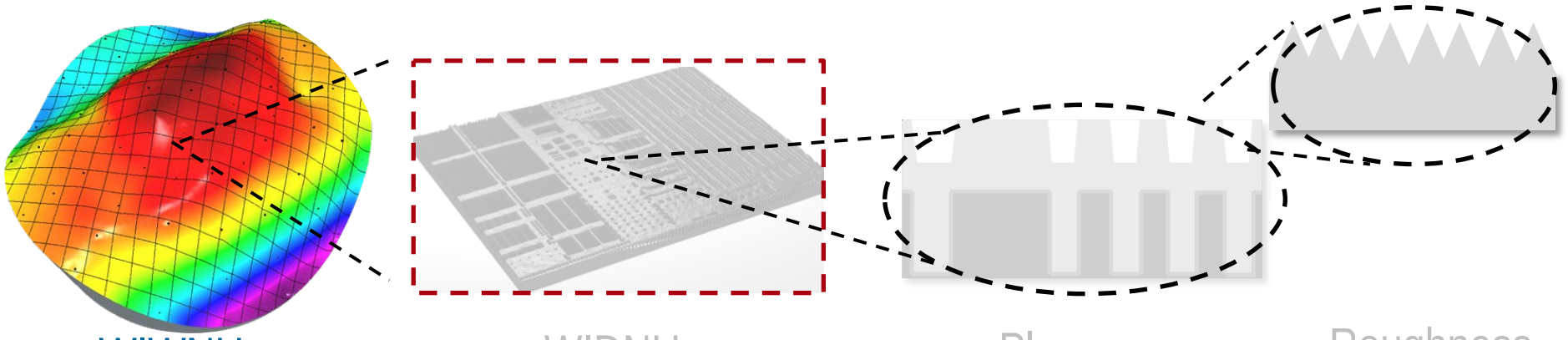
Post-CMP Low Topography ☺



Atomically Flattened Surfaces thru Design Optimization
→Excellent Hybrid Direct Bonding Quality

Chemical Mechanical Planarization

Challenges for Recreating The Bulk from 2 Surfaces



WIWNU

Diameter Planar

WIDNU

Die Planar

Planar

Device Planar

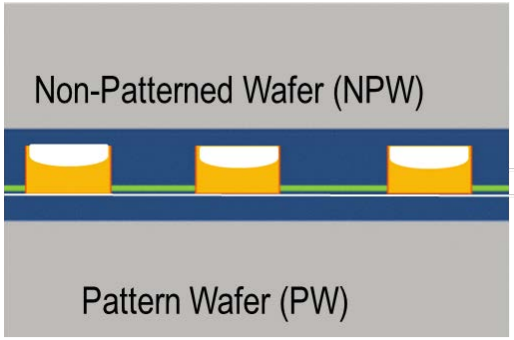
Roughness

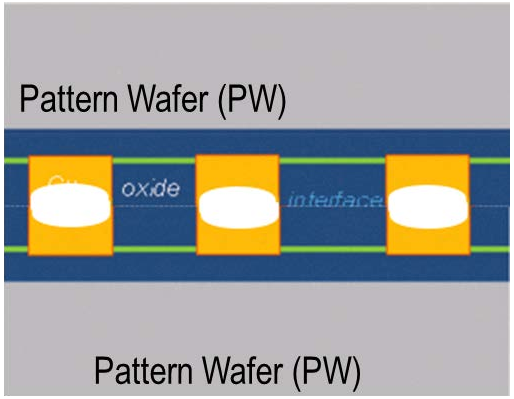
Atomic Planar

Hybrid Direct Bonding

Patterned Wafers DOE

- Pattern (PW) to non-patterned (NPW) bonding →
- → Validation Pattern to Pattern → 3 wafers/investigated point: 2 bonded, 1 characterized





Process Conditions Adjustement

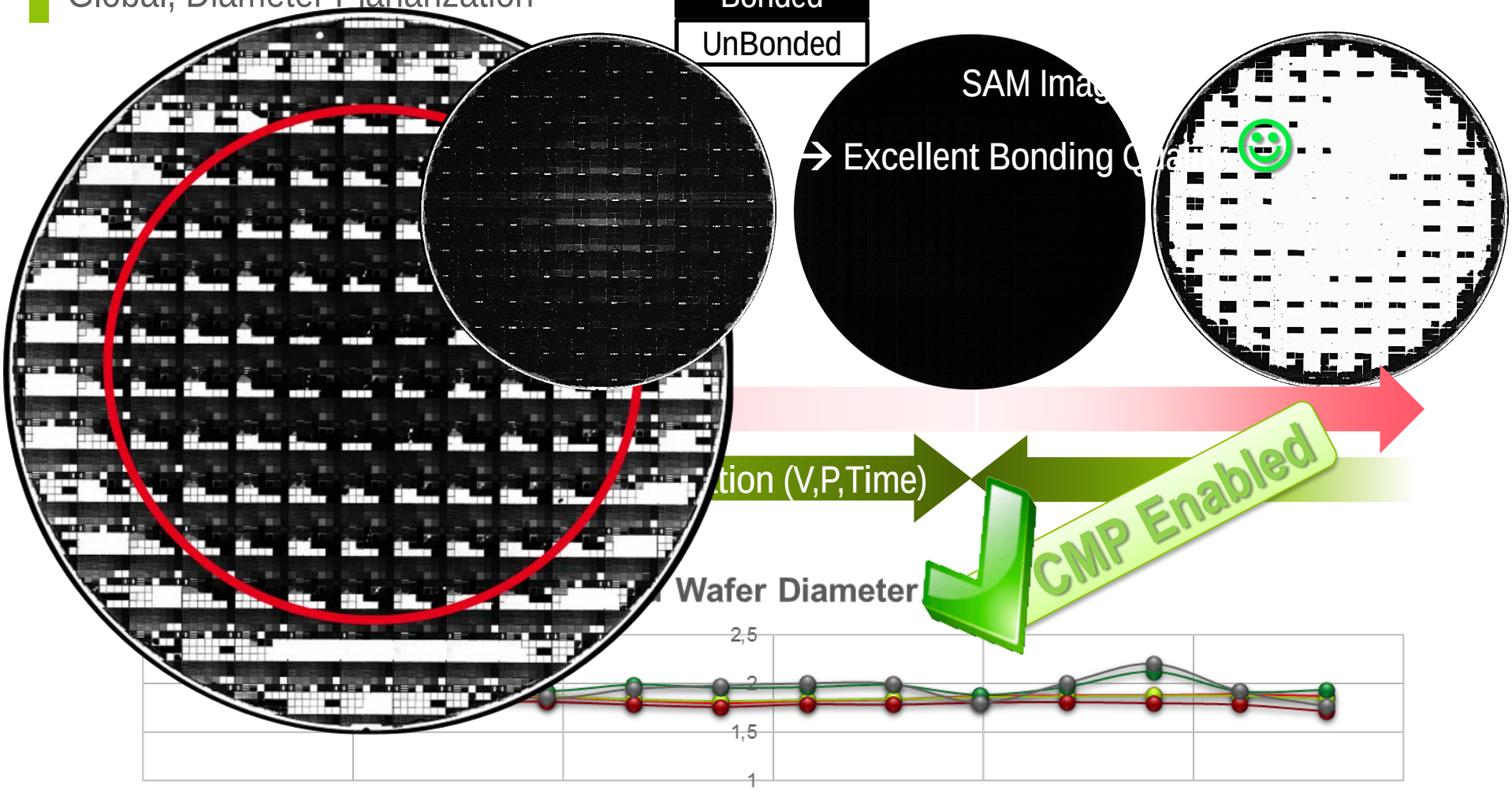
VP/Flow	Time	SiO2/Cu Selec	Post-CMP Topo	PW/NPW
h/a/z	a	a	c	
	b		a	
	c		b	
k/b/y	d	b	d	
	e		a	
k/c/y	f	c	e	
	e		a	
l/b/y	a	d	c	
	b		b	
l/c/y	b	e	c	
k/b/z	c	f	a	
	d		c	

Costly Process in Patterned Wafers

Stacking Heterogenous Devices

Dimension & Density Impact

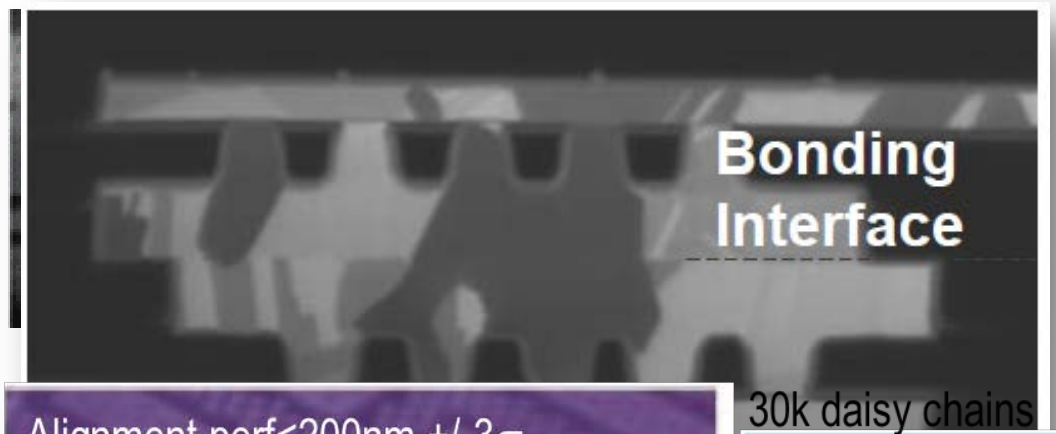
Global, Diameter Planarization

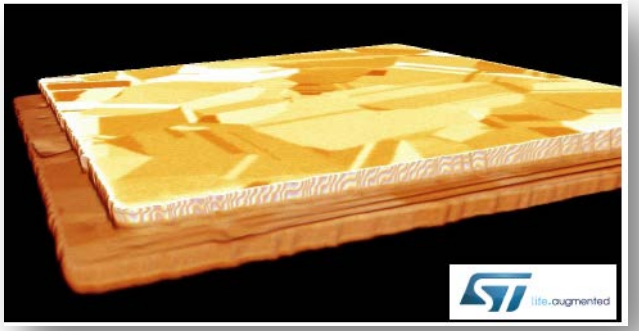


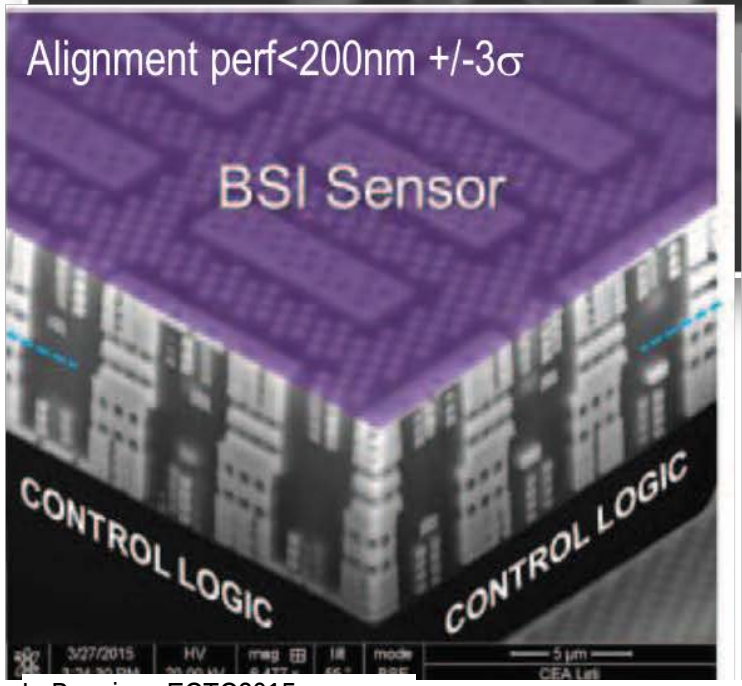
Improved Diameter Planarization through CMP Process Optimization, validated by Bonding Wave Propagation Time

Stacking Heterogenous Devices

Excellent Bonding: Bulk Reconstruction

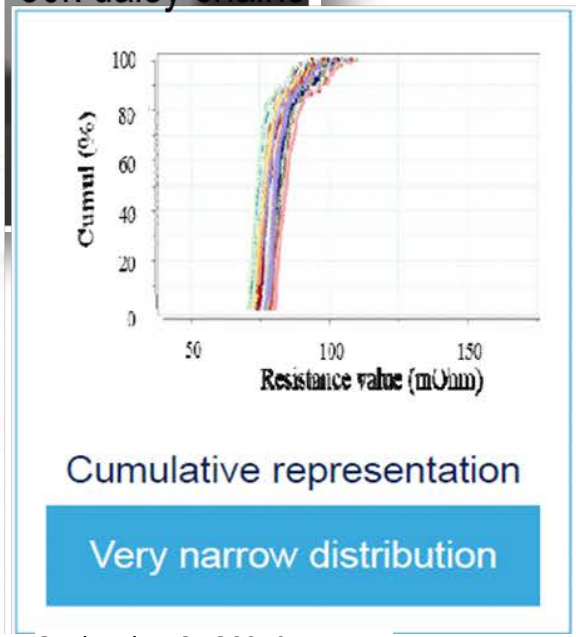


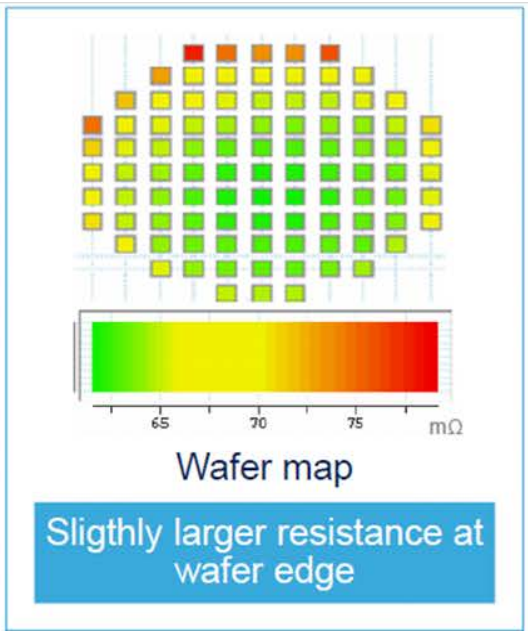




L. Benaissa ECTC2015

30k daisy chains



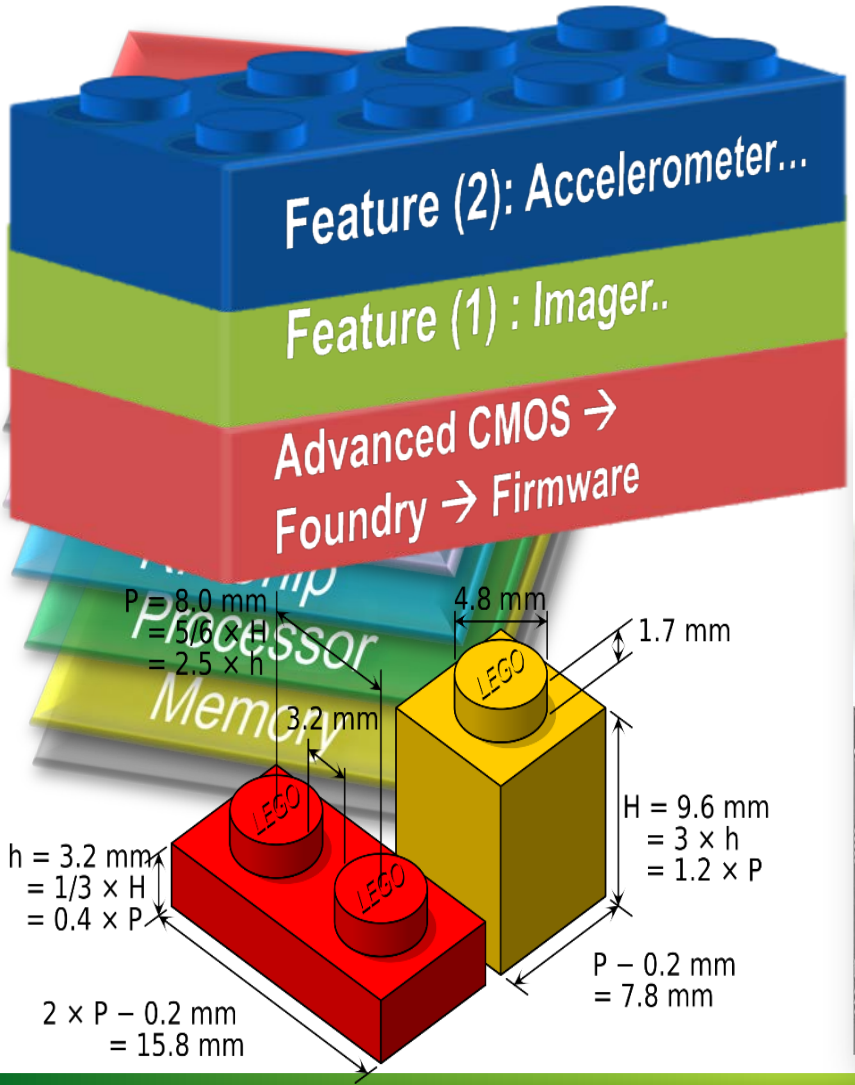


S. Lhostis ECTC2016

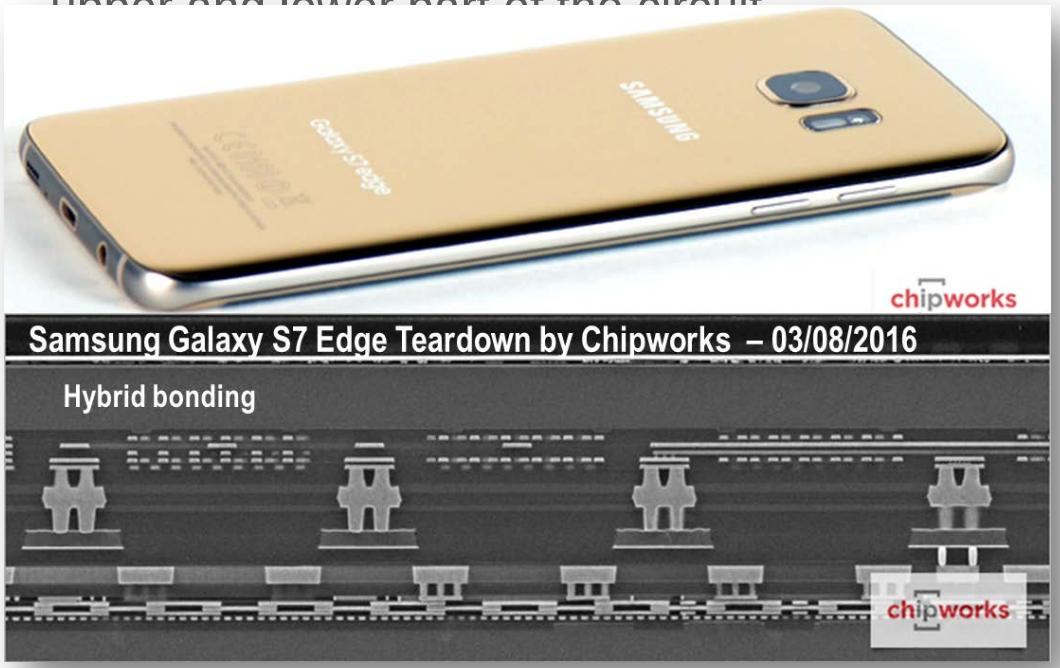
Copper Grain Reconstruction: Excellent Electrical Results, 100% Yield

Stacking Heterogenous Devices

Increase Device Cleverness



- 3D Stacking Heterogenous
  - ↘ Form Factor
  - ↘ Power consumption
  - ↗ Cleverness
- The key technology is the interconnection of the upper and lower part of the circuit



3D DieStore: Design Rules Standardization for Interconnect Level

Conclusion

3 Take-Home Messages

This Work was performed at STMicroelectronics conjointly with CEA-LETI, EVG and MCL.

Thanks to all the 3D integration team at STMicroelectronics and CEA-LETI.

This work was conceived within, and supported by “Pilot Optical Line for Imaging and Sensing” (POLIS), an ENIAC Joint Undertaking project.

Thank You

Leti, technology research institute
Commissariat à l’énergie atomique et aux énergies alternatives
Minatec Campus | 17 rue des Martyrs | 38054 Grenoble Cedex | France
www.leti.fr

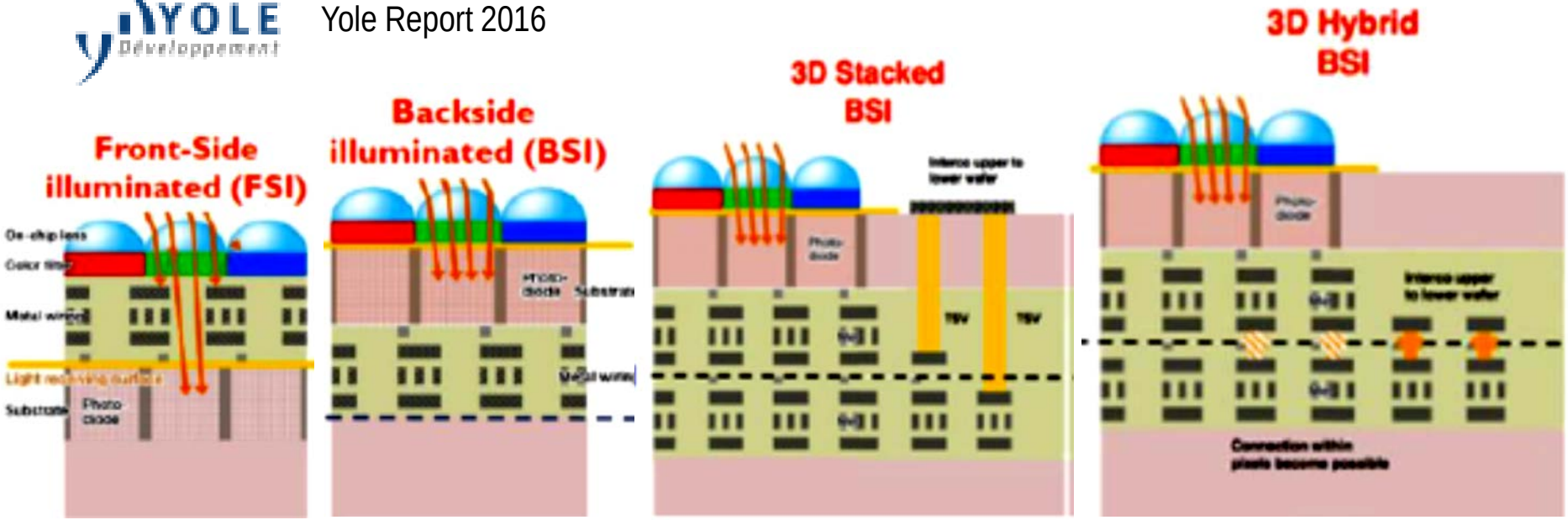
INSTITUT CARNOT CEA LETI


Design
CMP
Space is the Final Frontier

Image Sensor

Technology Evolution

Yole Report 2016



98% revenue in 2009

33% of the revenue in 2013

Currently TSV is the main technology to connect 3D stacked wafers.

Next Step → Cu-Cu Hybrid Bonding → Could open the way to in pixel connections