Chemical/Mechanical Balance Management through Pad Microstructure in CMP

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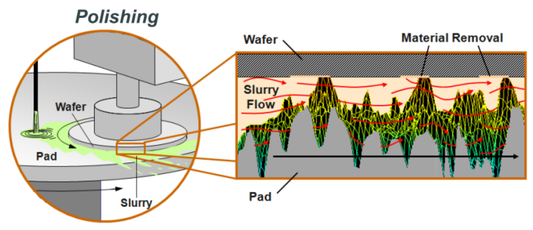
Introduction

CMP = SYNERGY between a **Chemical** and a **Mechanical** action

The slurry **chemically** modify the surface while the pad with the abrasive particles **mechanically** remove the modified surface. The **pad** plays a key role in the CMP process, it helps both the **chemical** and **mechanical** actions.



Pores + Grooves → Slurry Transport

Pores + Asperities → Wafer contact

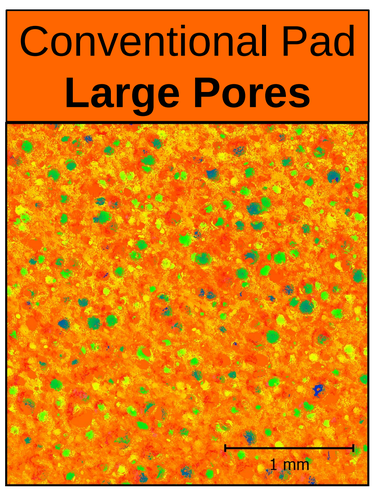
CMP

Pad's pores and grooves allow the **slurry transport** while the **contact with the wafer** is determined by its pores and asperities. In this study we focused on the **pores** which act on the two sides of the balance.

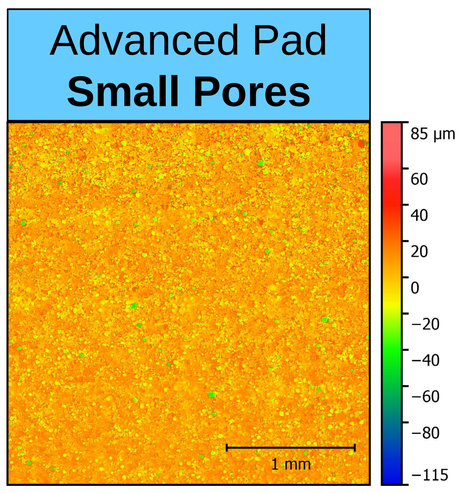
Experimental and Methodology

Blanket Si Wafers
polished on two kinds of
Pads with different pore sizes

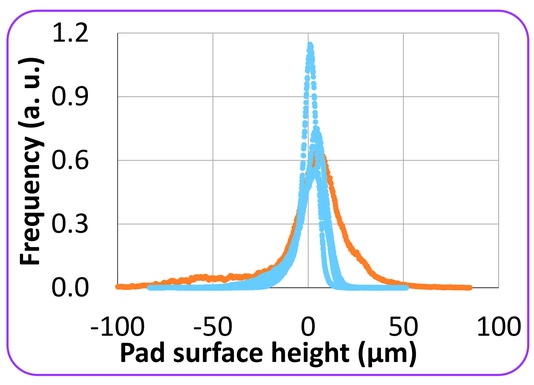
Conventional Pad
Large Pores



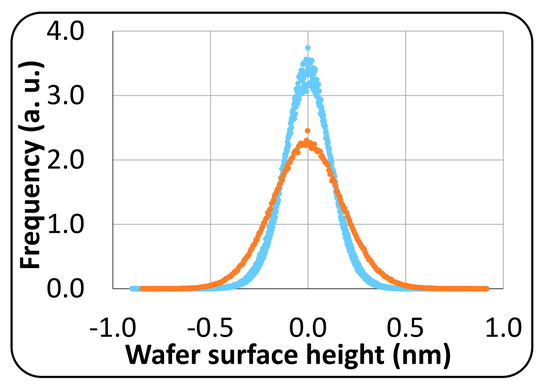
Advanced Pad
Small Pores



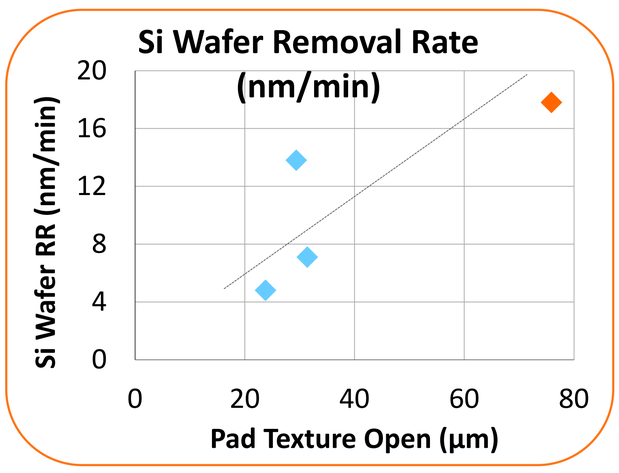
Pads Characterization :
- Roughness Parameters (Texture Open),
- Height Distributions
- Asperities Properties

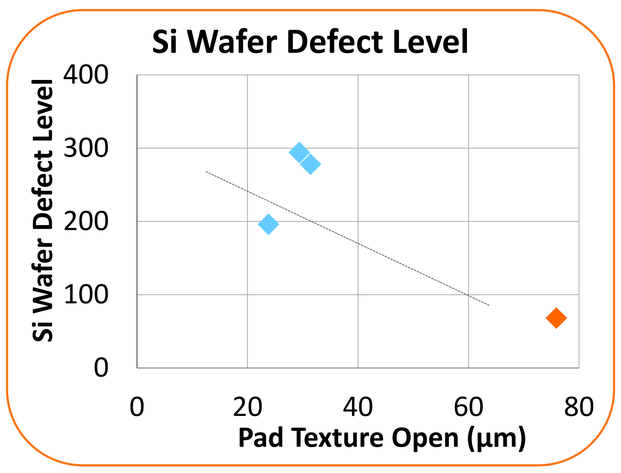


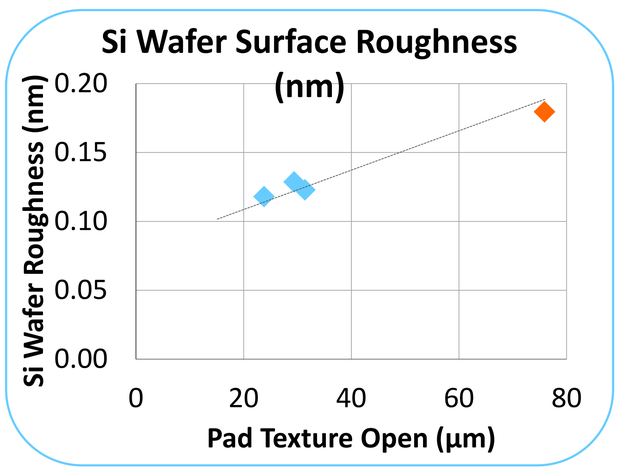
Wafers Characterization :
- Surface Roughness and Height Distributions (AFM),
- Defect Levels
- Si removal rates



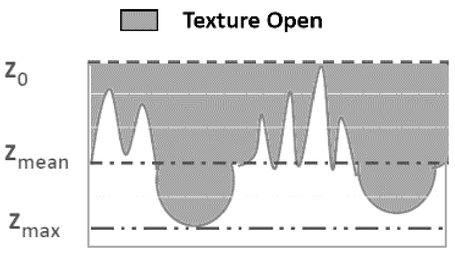
Results and Discussion







$$\text{Texture Open} = \frac{\text{Empty Volume}}{\text{Projected Area}}$$



As **Si CMP** is a more **chemical** process [1], removal rate is very dependent on **slurry transport ability** and consequently on texture open. **Higher pore size** increases the texture open and leads to **higher removal rate**.
Larger pores also allow a better evacuation of the byproducts, resulting in **better defect level**.
On the contrary, decreasing the texture open favor the **mechanical action** of the process, that's why the **planarization is better**.

Large pore size
→ **Higher RR & Lower Defectivity Level**

Small pore size
→ **Better Surface Roughness**

Chemical/Mechanical Balance can be managed through **Pad Microstructure.**
Advanced Pad & Wafer Characterization are required to better understand **Roughness Transfer from Pad to Wafer** and to achieve **better CMP Performances.**

[1] Y. Liu *et al.*, Microelectronic Engineering, Volume 66, Issues 1–4, April 2003, Pages 438-444