

Roadmap Past, Present and Future

Paolo Gargini

Chairman ITRS2.0

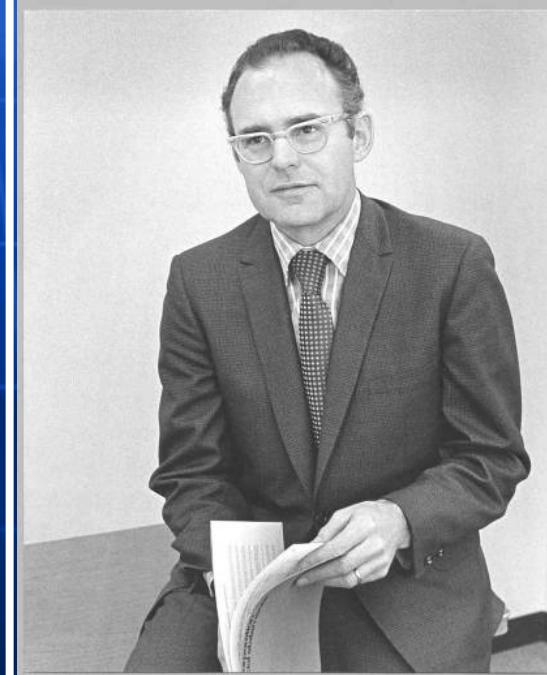
Fellow IEEE, Fellow I-JSAP

Intel Fellow (1995-2012)

Multiple Stories

1. **Introduction**
2. 1998. ITRS 1.0
 1. Equivalent Scaling
3. 2000. NNI.
4. 2005. Nanoelectronics Research Initiative (NRI)
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13. 2017-2021. 3D POWER Scaling

Second Update of Moore's Law



International Electron Device Meeting, December 1975

Dennard Scaling

Device or Circuit Parameter	Scaling Factor
Device dimension t_{ox} , L, W	$1/K$
Doping concentration N_A	K
Voltage V	$1/K$
Current I	$1/K$
Capacitance eA/t	$1/K$
Delay time per circuit VC/I	$1/K$
Power dissipation per circuit VI	$1/K^2$
Power density VI/A	1

Dennard's 1974 paper summarizes transistor or circuit parameter changes under ideal MOSFET device scaling conditions, where K is the unitless scaling constant.

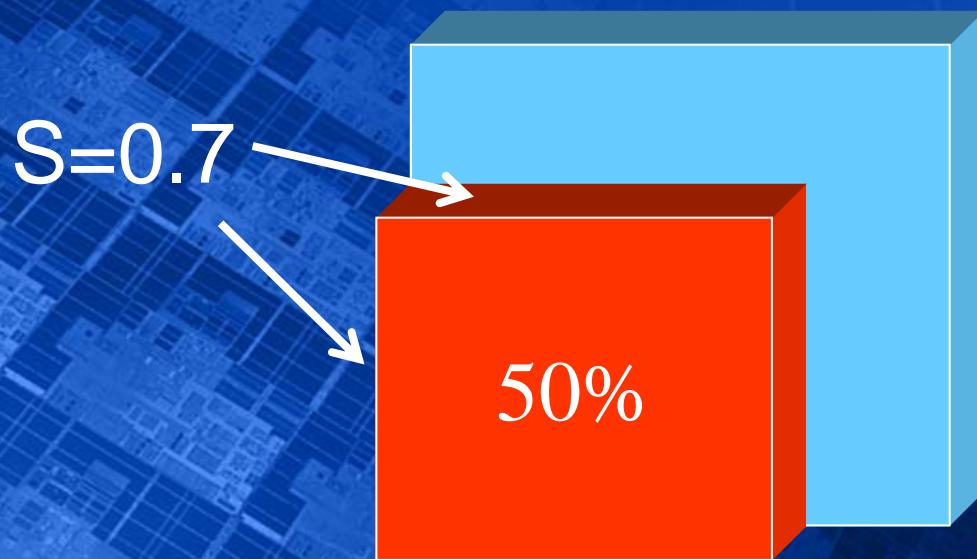
The benefits of scaling : as transistors get smaller, they can switch faster and use less power. Each new generation of process technology was expected to reduce minimum feature size by approximately 0.7x ($K \sim 1.4$). A 0.7x reduction in linear features size provided roughly a 2x increase in transistor density.

Dennard scaling broke down around 2004 with unscaled interconnect delays and our inability to scale the voltage and the current due to reliability concerns.

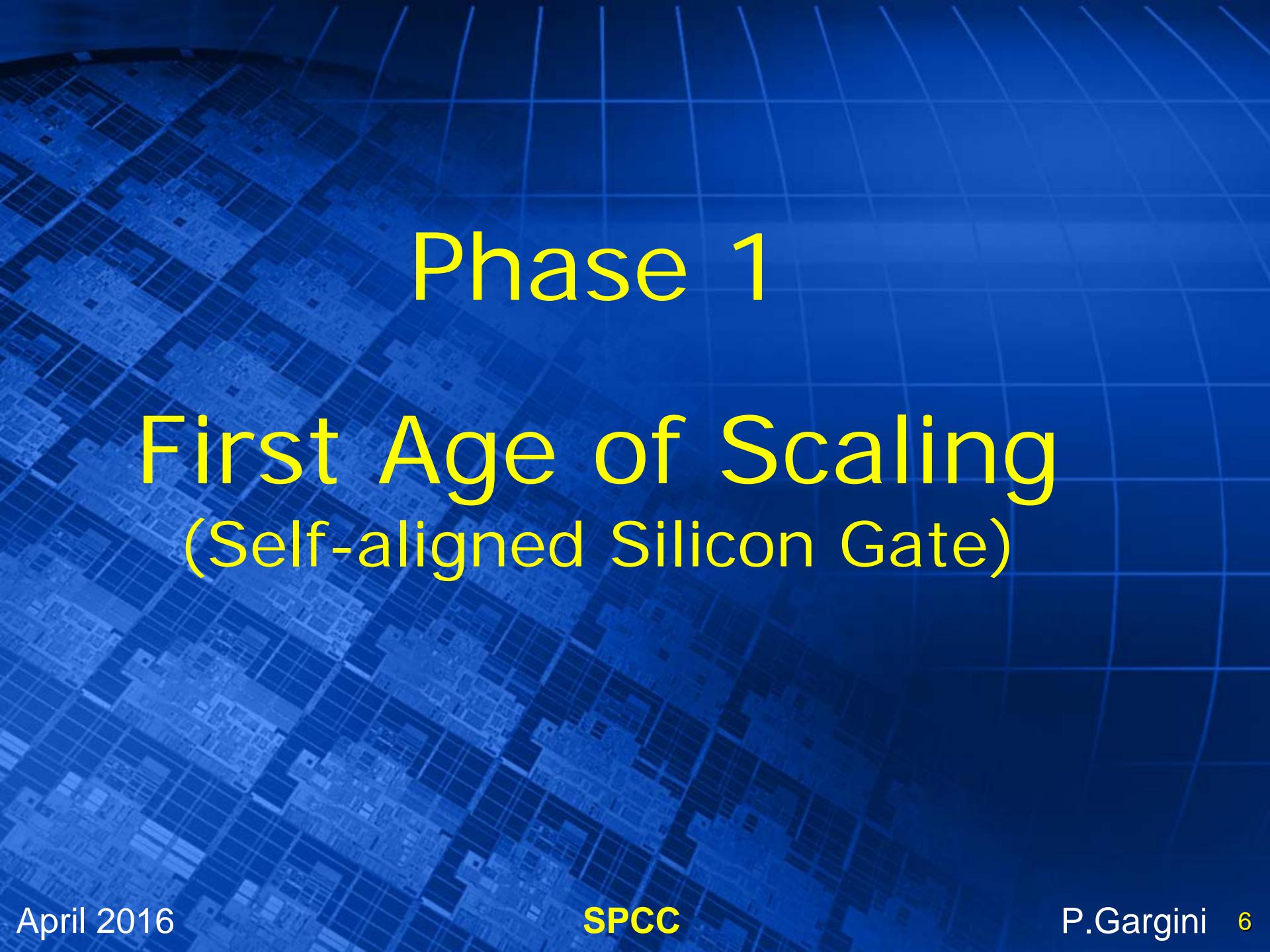
But our the ability to etch smaller transistors has continued spawning multicore designs.

Moore's Law and Dennard's Scaling Laws Convergence

=> 30% LINEAR FEATURE REDUCTION



50% AREA REDUCTION
GENERATION TO GENERATION



Phase 1

First Age of Scaling (Self-aligned Silicon Gate)

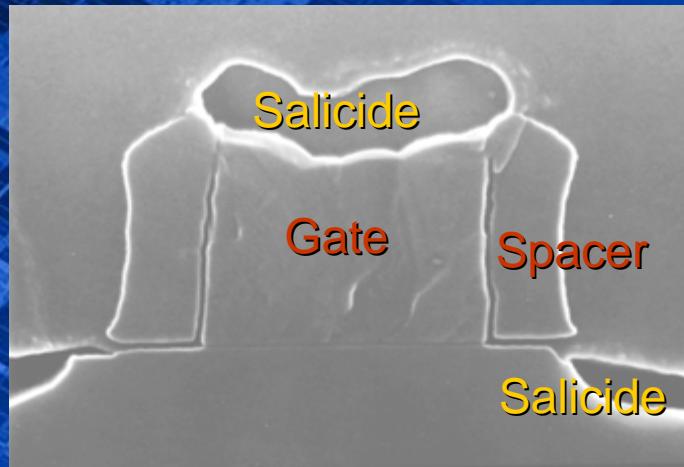
IC Industry at a Glance (1975-2003)

Driver → Cost/transistor -> 50% Reduction

How → 2x Density/2 years (Moore)

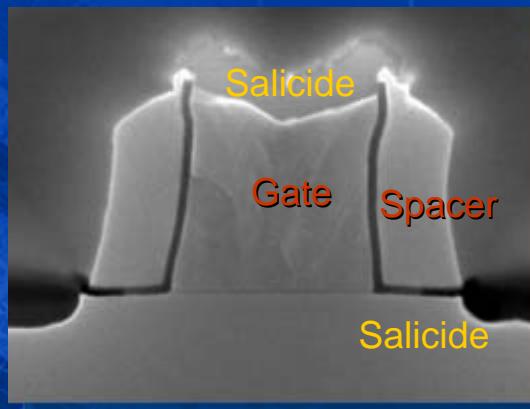
Method → Geometrical Scaling (Dennard)

The Incredible Shrinking Silicon Technology of the 90's



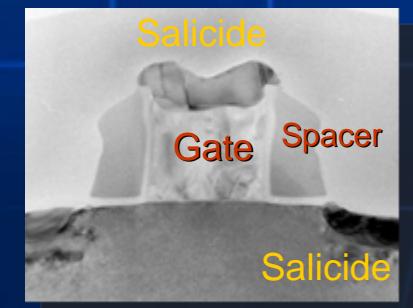
0.35μ

1995



0.25μ

1997



0.18μ

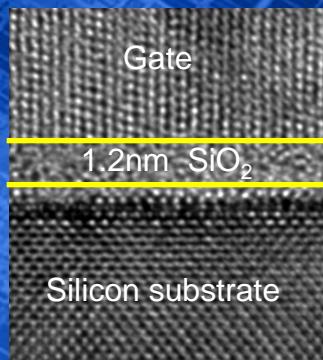
1999

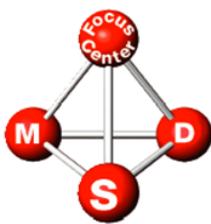


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Gate Dielectric Scaling





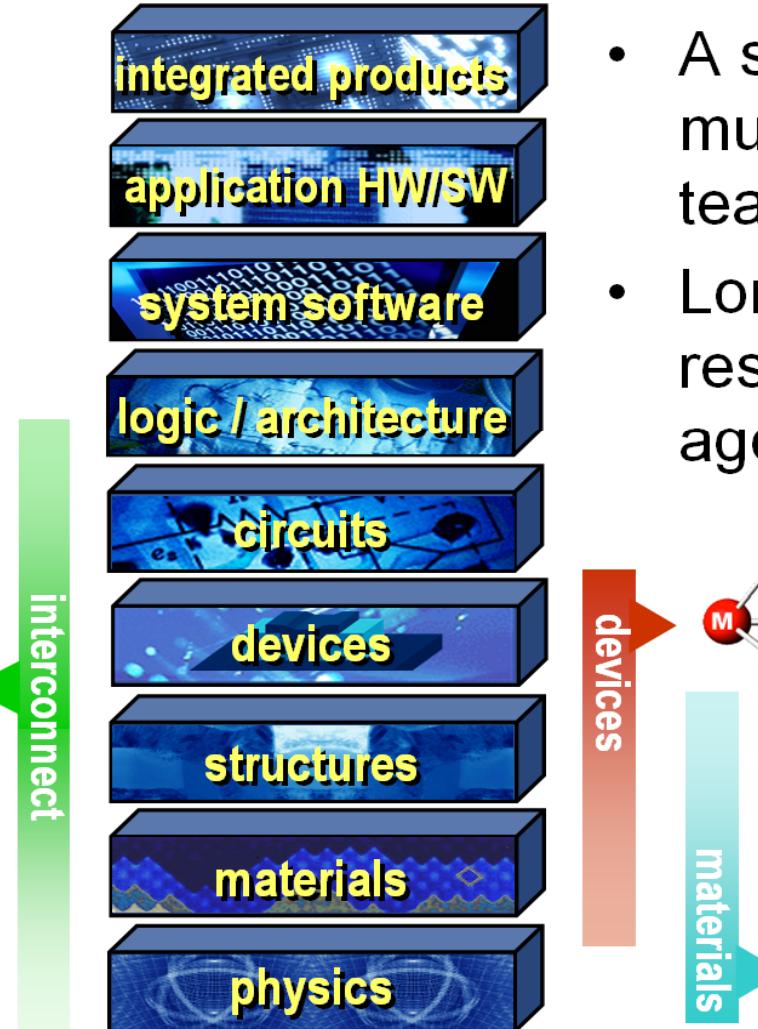
The Focus Center Research Program



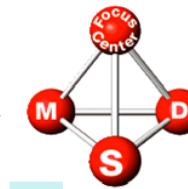
interconnect
focus center

systems

circuits



- A set of national multi-university teams
- Long-range research vision & agendas



Semiconductor Industry
Association



DUSD(LABS)



Multiple Stories

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1998 ITRS Update

- Participation extended to: EECA, EIAJ, KSIA, TSIA at WSC on April 23,1998
- 1st Meeting held on July 10/11,1998 in San Francisco
- 2nd meeting held on December 10/11,1998 at SFO
- 50% of tables in 1997 NTRS required some changes
- 1998 ITRS Update posted on web in April 1999



ITRS 1.0



1998

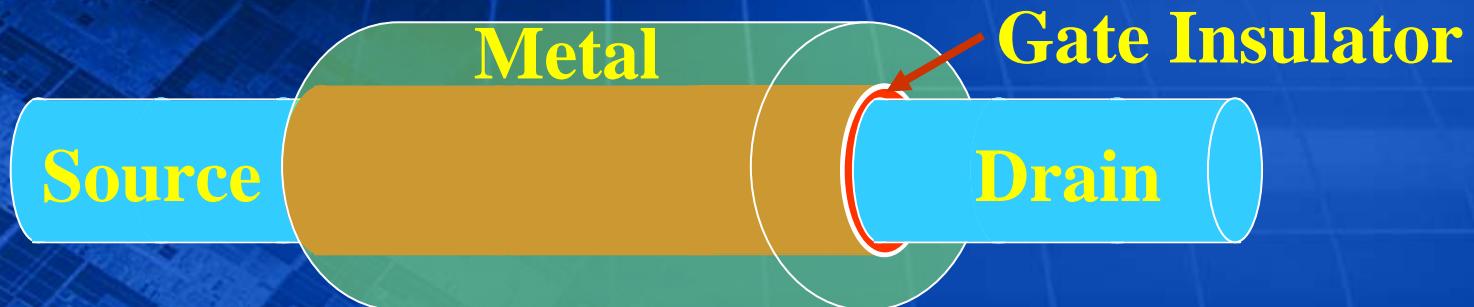
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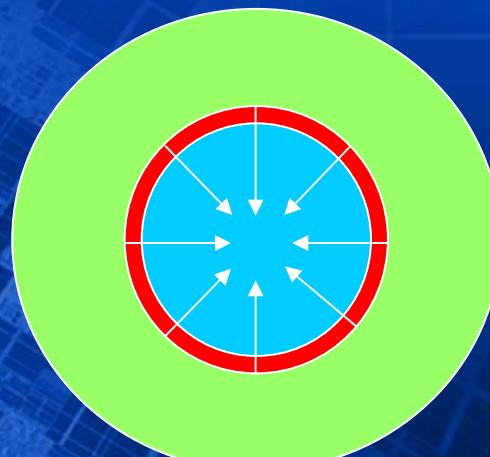
Phase 2

Second Age of Scaling (Equivalent Scaling)

The Ideal MOS Transistor



Fully Surrounding
Metal Electrode



Fully Enclosed,
Depleted
Semiconductor

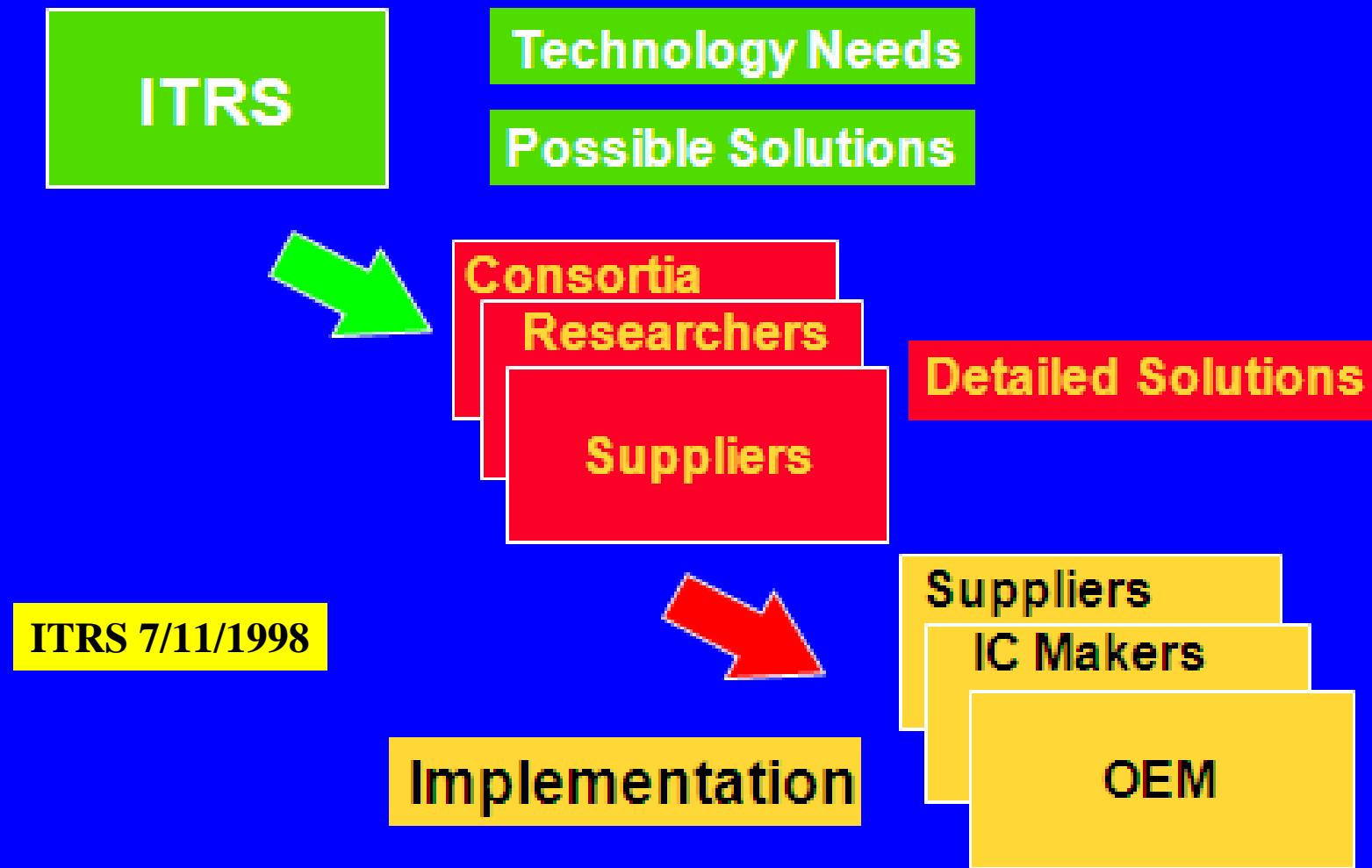
High-K
Gate Insulator

Band Engineered
Semiconductor

Low Resistance
Source/Drain

From My Files

From Strategy to Implementation



International Technology Roadmap for Semiconductors

P.Gargini

IC Industry at a Glance (2003->2021)

- Driver → Cost/transistor-> 50% Reduction
- How → 2x Density/2 years (Moore)
- Method → Equivalent Scaling (ITRS1.0)

The Start of the ITRS

<http://www.itrs2.net>

1991
Micro Tech 2000
Workshop Report

1992NTRS

1994NTRS

1997NTRS

Europe

Japan

Korea

Taiwan

USA

1998 ITRS
Update

1999 ITRS

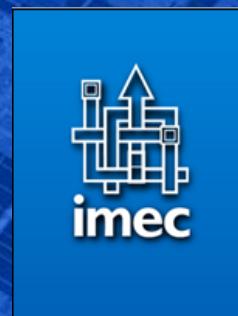
2000 ITRS
Update

2001 ITRS

2002 ITRS
Update

High-k/Metal-Gate

(year 2000)



SRC/ISMT Front End Processes Research Center

Transistor Innovations Enable Technology Cadence



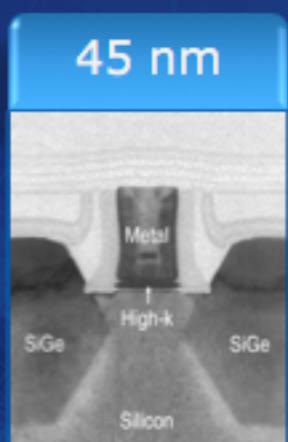
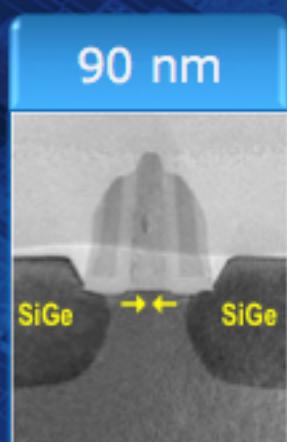
2003

2005

2007

2009

2011



SiGe
Strained Silicon

2nd Gen.
SiGe
Strained Silicon

Gate-Last
High-k Metal Gate

2nd Gen.
Gate-Last
High-k Metal Gate

Strained Silicon

High k Metal gate

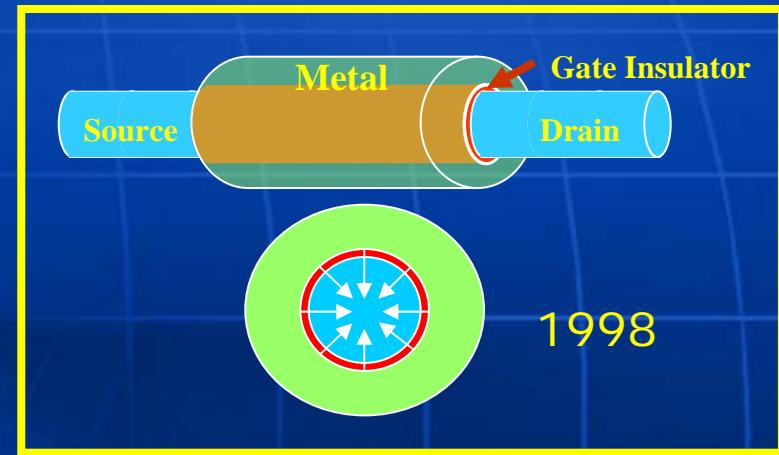
Four year pace of introduction of Equivalent Scaling into production

Source: Intel

Tri-Gate

Incubation Time

	Early Invention	Focused Research	Introduction Manufacturing
Strained Silicon	1992	1998	2003
HKMG	1996	1998	2007
Raised S/D	1993	1998	2009
MultiGates	1988	2000	2011



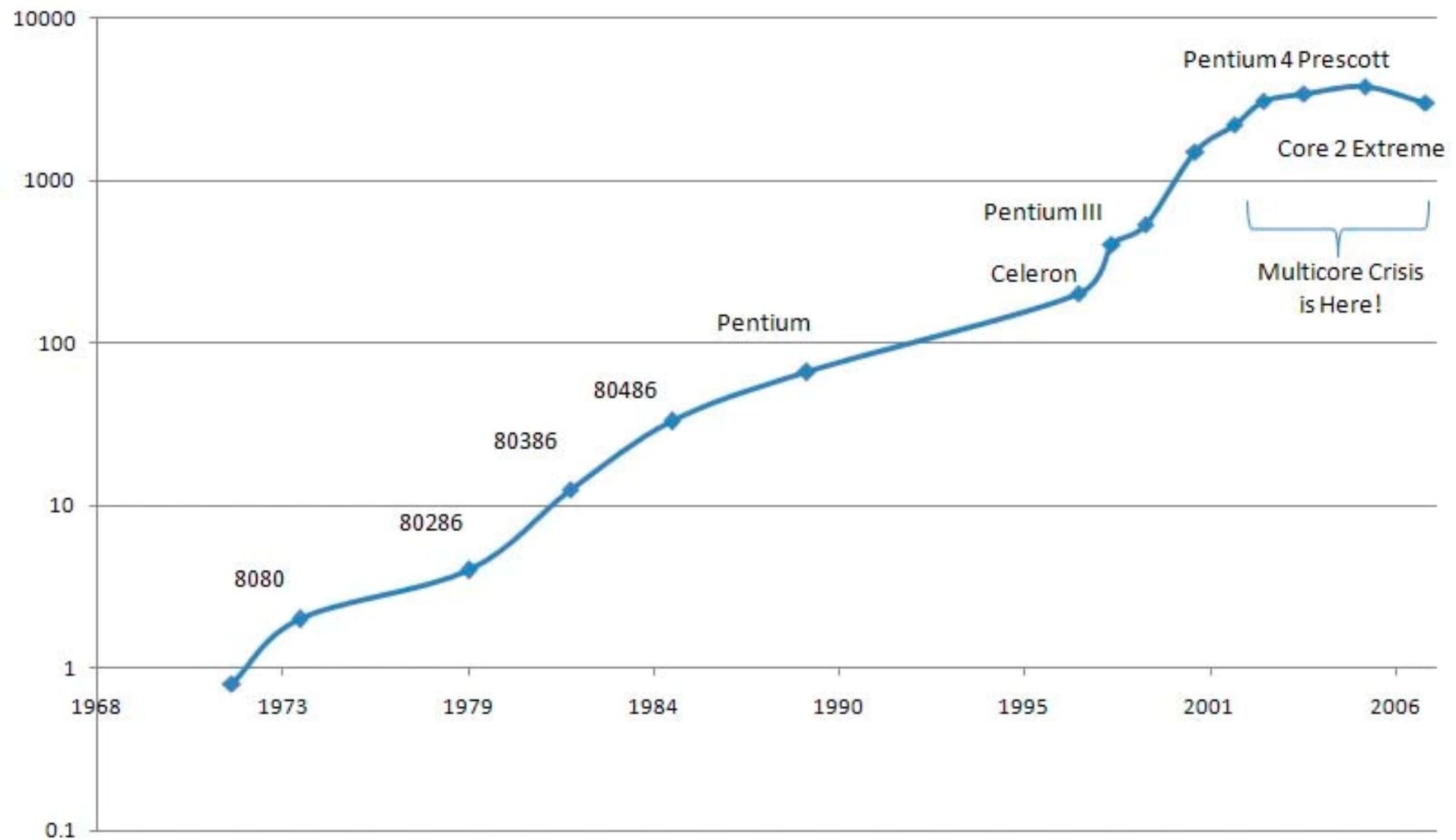
<11 years

Sortable table

Model	Core	Clock Speed	Thermal Design Power
Pentium 4 1.3	Willamette (180 nm)	1.3 GHz	51.6 W
Pentium 4 1.4 (Socket 423)	Willamette (180 nm)	1.4 GHz	54.7 W
Pentium 4 1.4 (Socket 478)	Willamette (180 nm)	1.4 GHz	55.3 W
Pentium 4 1.5 (Socket 423)	Willamette (180 nm)	1.5 GHz	57.8 W
Pentium 4 1.5 (Socket 478)	Willamette (180 nm)	1.5 GHz	57.9 W
Pentium 4 1.6 (Socket 423)	Willamette (180 nm)	1.6 GHz	61 W
Pentium 4 1.6 (Socket 478)	Willamette (180 nm)	1.6 GHz	60.8 W
Pentium 4 1.7 (Socket 423)	Willamette (180 nm)	1.7 GHz	64 W
Pentium 4 1.7 (Socket 478)	Willamette (180 nm)	1.7 GHz	63.5 W
Pentium 4 1.8 (Socket 423)	Willamette (180 nm)	1.8 GHz	66.7 W
Pentium 4 1.8 (Socket 478)	Willamette (180 nm)	1.8 GHz	66.1 W
Pentium 4 1.9 (Socket 423)	Willamette (180 nm)	1.9 GHz	69.2 W
Pentium 4 1.9 (Socket 478)	Willamette (180 nm)	1.9 GHz	72.8 W

Pentium 4 HT 560	Prescott (90 nm)	3.6 GHz	115 W
Pentium 4 HT 560J	Prescott (90 nm)	3.6 GHz	115 W
Pentium 4 HT 561	Prescott (90 nm)	3.6 GHz	115 W

Intel Processor Clock Speed (MHz)

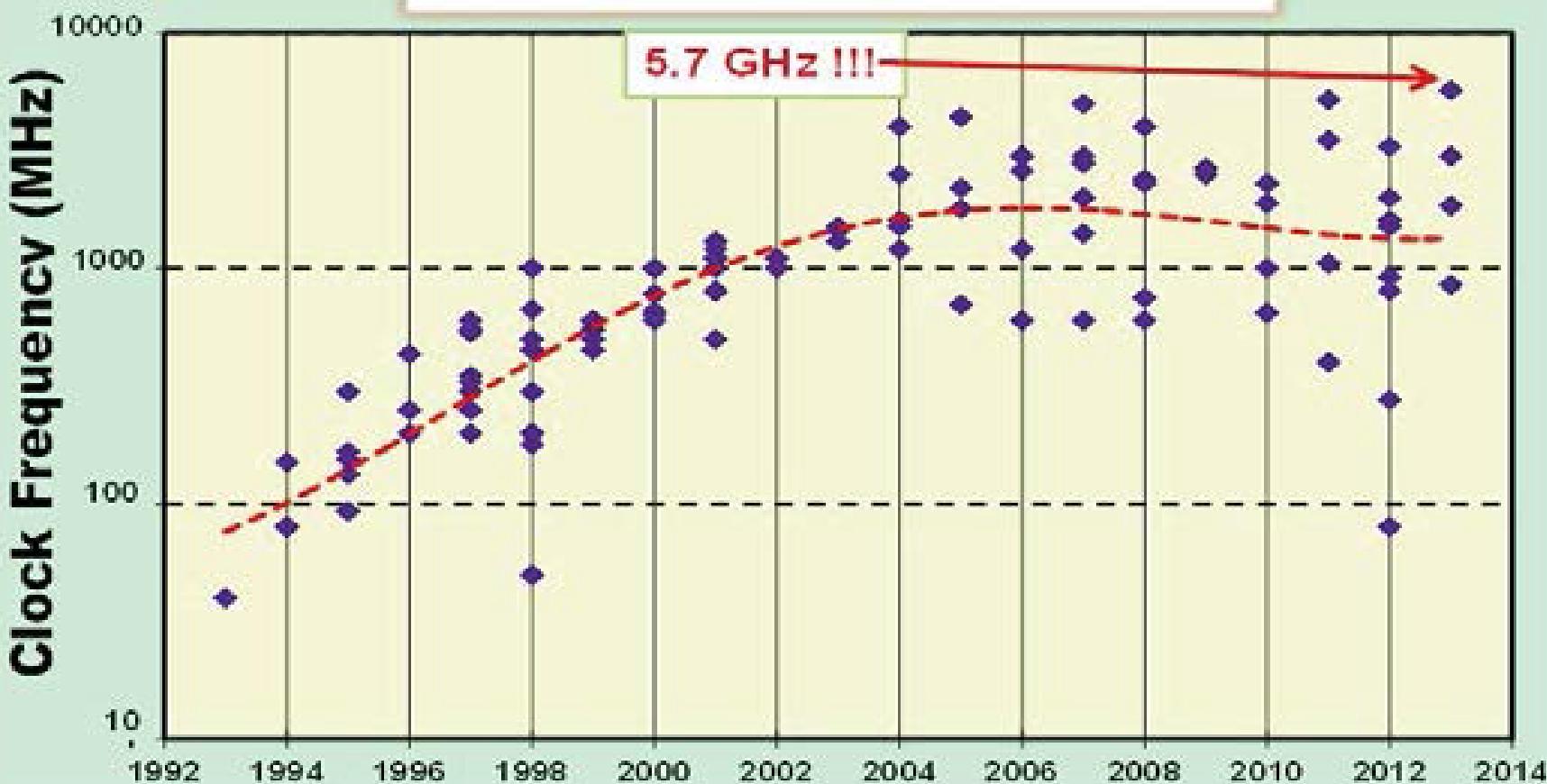


Sortable table

Model	Core	Clock Speed	Thermal Design Power
Core 2 Duo E4200	Conroe (65 nm)	1.6 GHz	65 W
Core 2 Duo E4300	Conroe (65 nm)	1.8 GHz	65 W
Core 2 Duo E4400	Conroe (65 nm)	2 GHz	65 W
Core 2 Duo E4500	Conroe (65 nm)	2.2 GHz	65 W
Core 2 Duo E4600	Conroe (65 nm)	2.4 GHz	65 W
Core 2 Duo E4700	Conroe (65 nm)	2.6 GHz	65 W

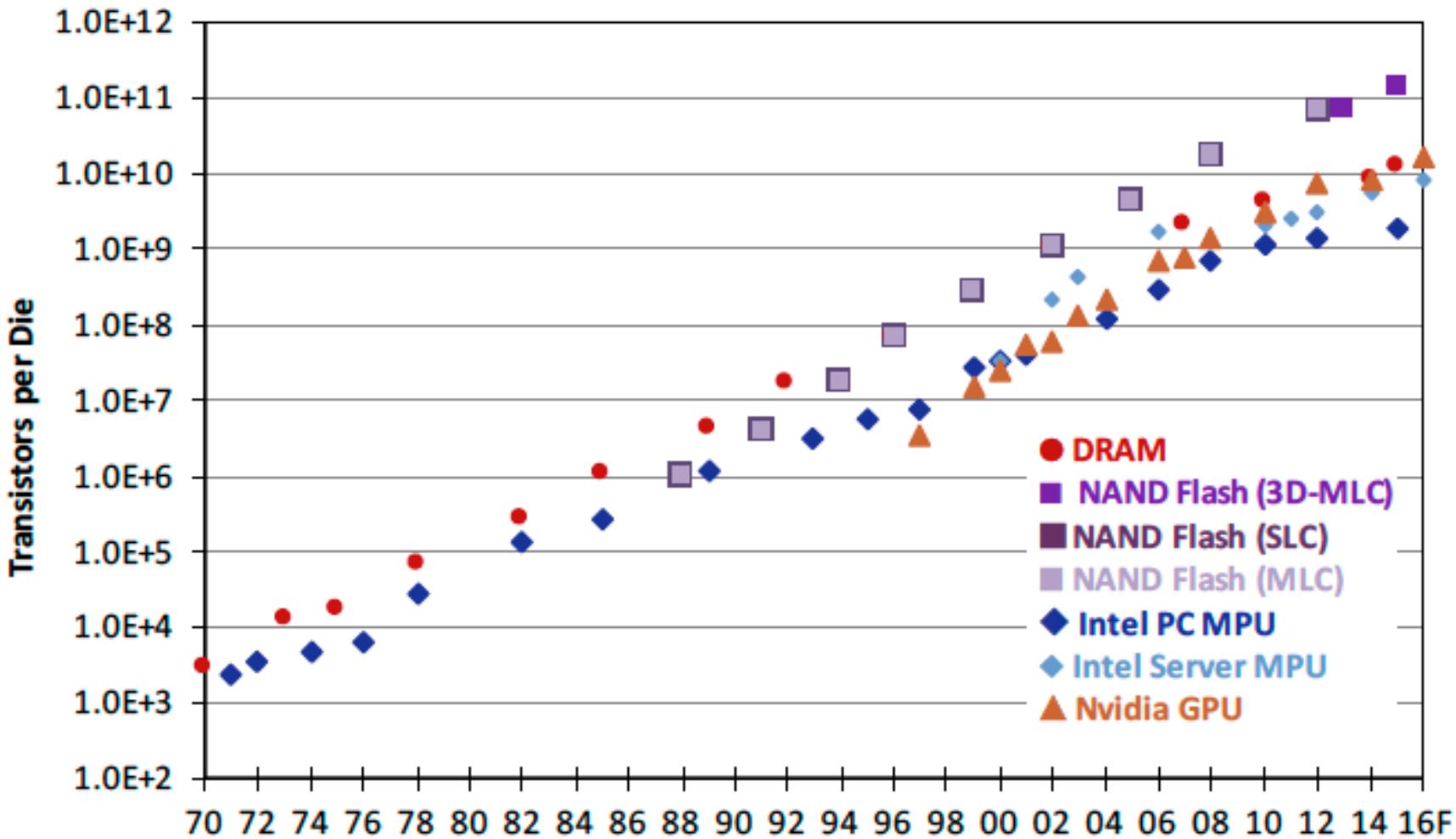
Core 2 Duo E8190	Wolfdale (45 nm)	2.66 GHz	65 W
Core 2 Duo E8200	Wolfdale (45 nm)	2.66 GHz	65 W
Core 2 Duo E8300	Wolfdale (45 nm)	2.83 GHz	65 W
Core 2 Duo E8400	Wolfdale (45 nm)	3 GHz	65 W
Core 2 Duo E8500	Wolfdale (45 nm)	3.16 GHz	65 W
Core 2 Duo E8600	Wolfdale (45 nm)	3.33 GHz	65 W

CLOCK FREQUENCY



IEEE, ISSCC: Transistor's 60th year commemorative supplement

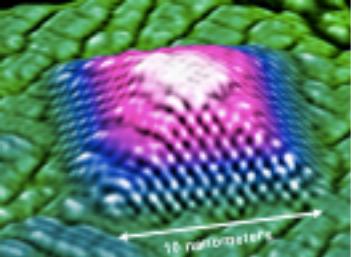
Transistor Count Trends



Sources: Intel, SIA, Wikipedia, IC Insights

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National Nanotechnology Initiative (NNI)

“My budget supports a major new National Nanotechnology Initiative, worth \$500 million.... the ability to manipulate matter at the atomic and molecular level. Imagine the possibilities: materials with ten times the strength of steel and only a small fraction of the weight -- shrinking all the information housed at the Library of Congress into a device the size of a sugar cube -- detecting cancerous tumors when they are only a few cells in size. Some of our research goals may take 20 or more years to achieve, but that is precisely why there is an important role for the federal government.”

--President William J. Clinton

January 21, 2000

California Institute Of Technology

NRI Funded Universities



Finding the Next Switch



Notre Dame Illinois-UC Michigan Cornell

Purdue
Penn State
UT-Dallas
GIT



SUNY-Albany GIT
Purdue RPI
Caltech MIT
Yale UVA

Harvard
Columbia
NCSU



Western
Institute of
Nanoelectronics

- UC Los Angeles
- C Berkeley
- UC Irvine
- UC Santa Barbara
- Stanford
- U Denver
- Portland State
- U Iowa



SWAN

Southwest Academy of Nanoelectronics

UT-Austin
UT-Dallas
U. Maryland

Rice
ASU
NCSU

Texas A&M Notre Dame Illinois UC

Over 30 Universities in 20 States

SPCC

Nanoelectronics: An International Perspective

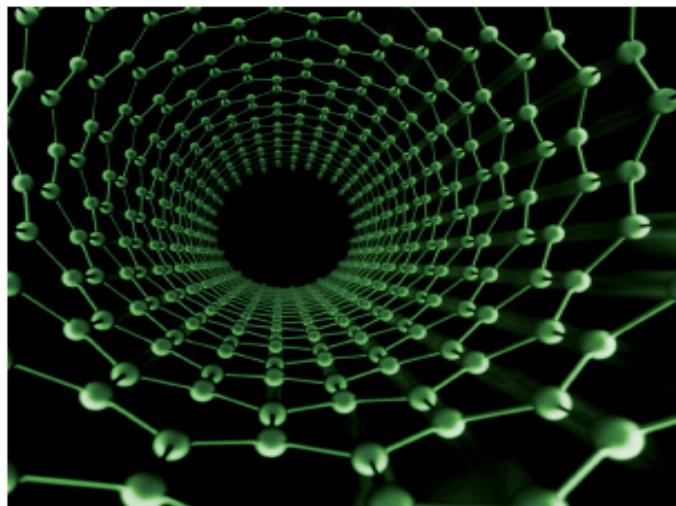
By MIHAEL C. ROCO

NSF and NNI

PAOLO GARGINI

ITRS Chairman

Intel



Discoveries and innovations in nanotechnology are flourishing worldwide. Centers of excellence and research networks with long term programs supporting nanoelectronics, nanomagnetics, and nanophotonics have been created in the United States (U.S.), Europe, Japan, and other parts of the world. The National Nanotechnology Initiative (NNI) has provided a long-term scientific focus, a partnership approach, and a means of environmentally responsible funding the field in the United States since 2000. The program also inspired and partially motivated nanotechnology R&D activities in about 60 other countries. Creative

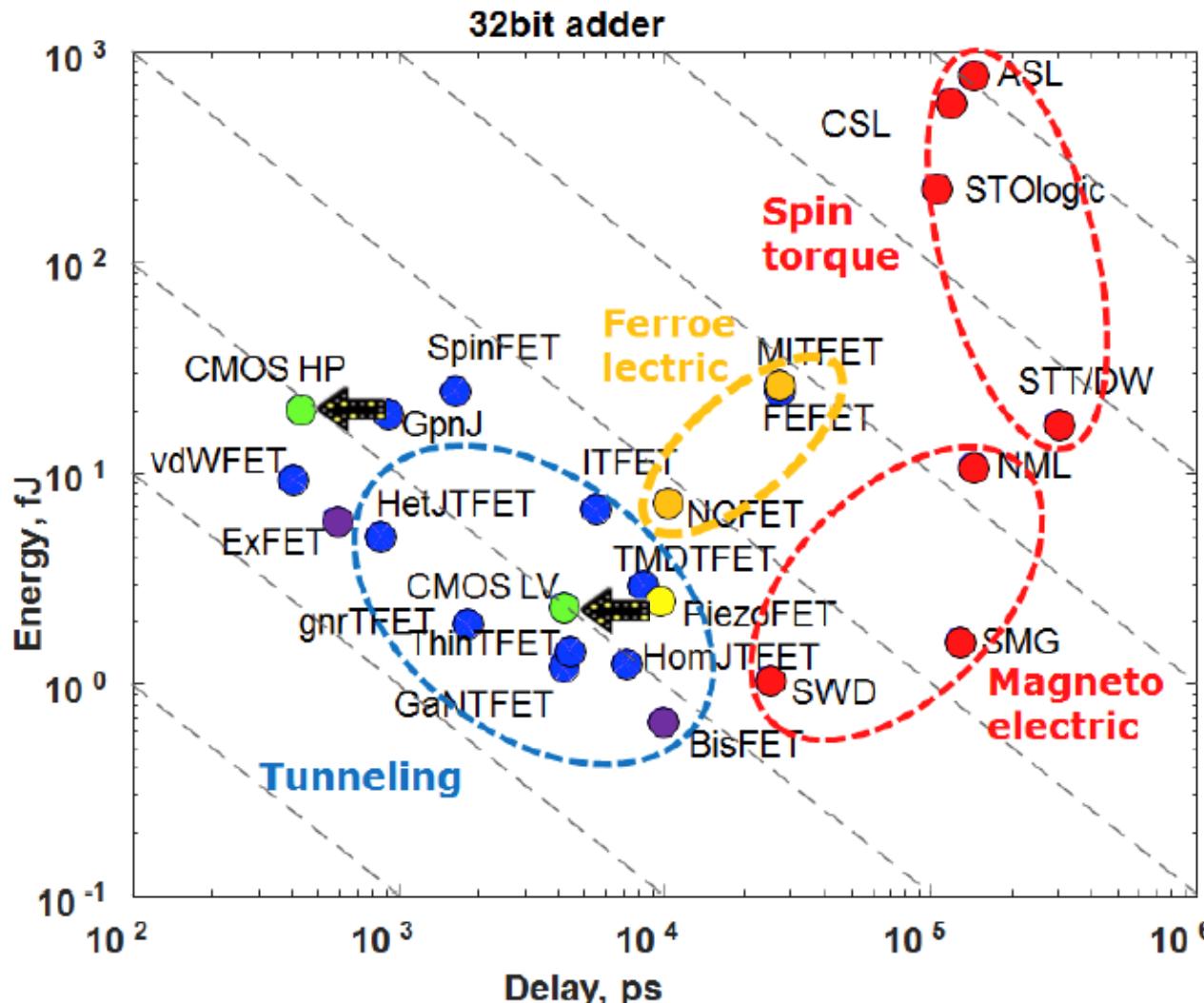
programs of similar investment scale are underway in Europe and Asia. In Europe, the FP7 program organizes all the EU research initiatives including in nanoelectronics into four categories: Cooperation, Ideas, People, and Capacities. For each objective, there is a specific program corresponding to the main areas of EU research policy. In addition, a European Commission program in Future Emerging Technologies (FET) addresses the disruptive approaches to nanoelectronics. In Japan, the Ministry of Education, Culture, Sports, Science, and Technology (MEXT) promotes nanotechnology research and development and supports a network among researchers to provide cross-sectional, comprehensive support across research institutions and research fields. For example, MEXT also provides opportunities for outside researchers to use large and special facilities and equipment. Japan also has the New Energy and Industrial Technology Development Organization (NEDO), which contributes research and development activities in a variety of nanoelectronic programs, e.g., their Next-Generation Semiconductor Materials and Process Technology (MIRAI) Project.

In the first ten years, the research focus in the U.S. has been on uncovering nanoscale phenomena and on synthesizing nanostructured components to improve existing products. For illustration, researchers and manufacturers have placed functional

Nanoelectronics Research Initiative

Benchmarking of Beyond-CMOS Exploratory Devices for Logic Integrated Circuits

Dmitri E. Nikonov and Ian A. Young, 2015, IEEE J. on Exploratory Solid-State Computational Devices and Circuits



Switching energy vs. delay of a 32-bit adder

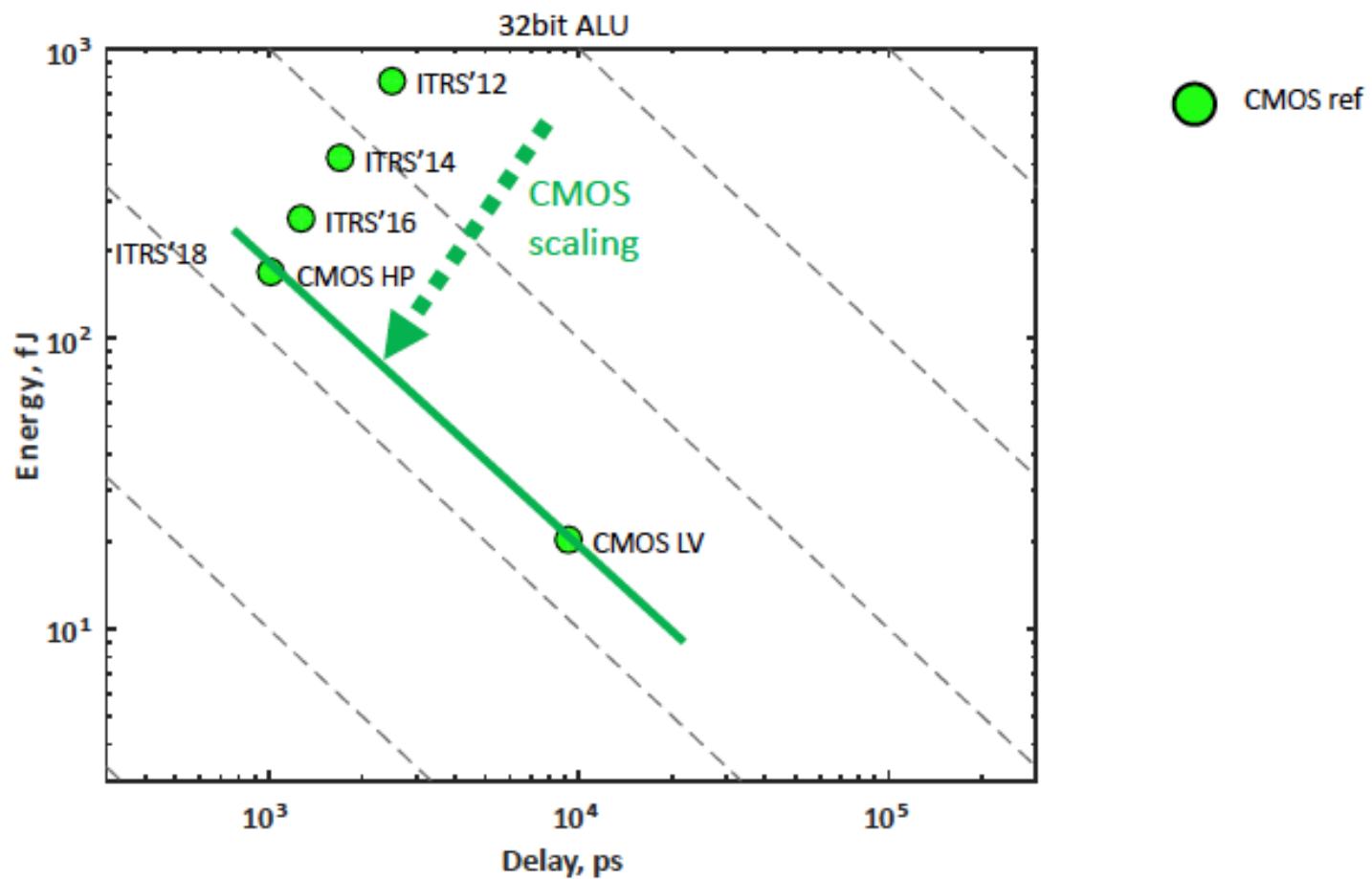
Moore's Law: A Path Forward

Bill Holt

Executive Vice President, Intel
General Manager, Technology and Manufacturing Group

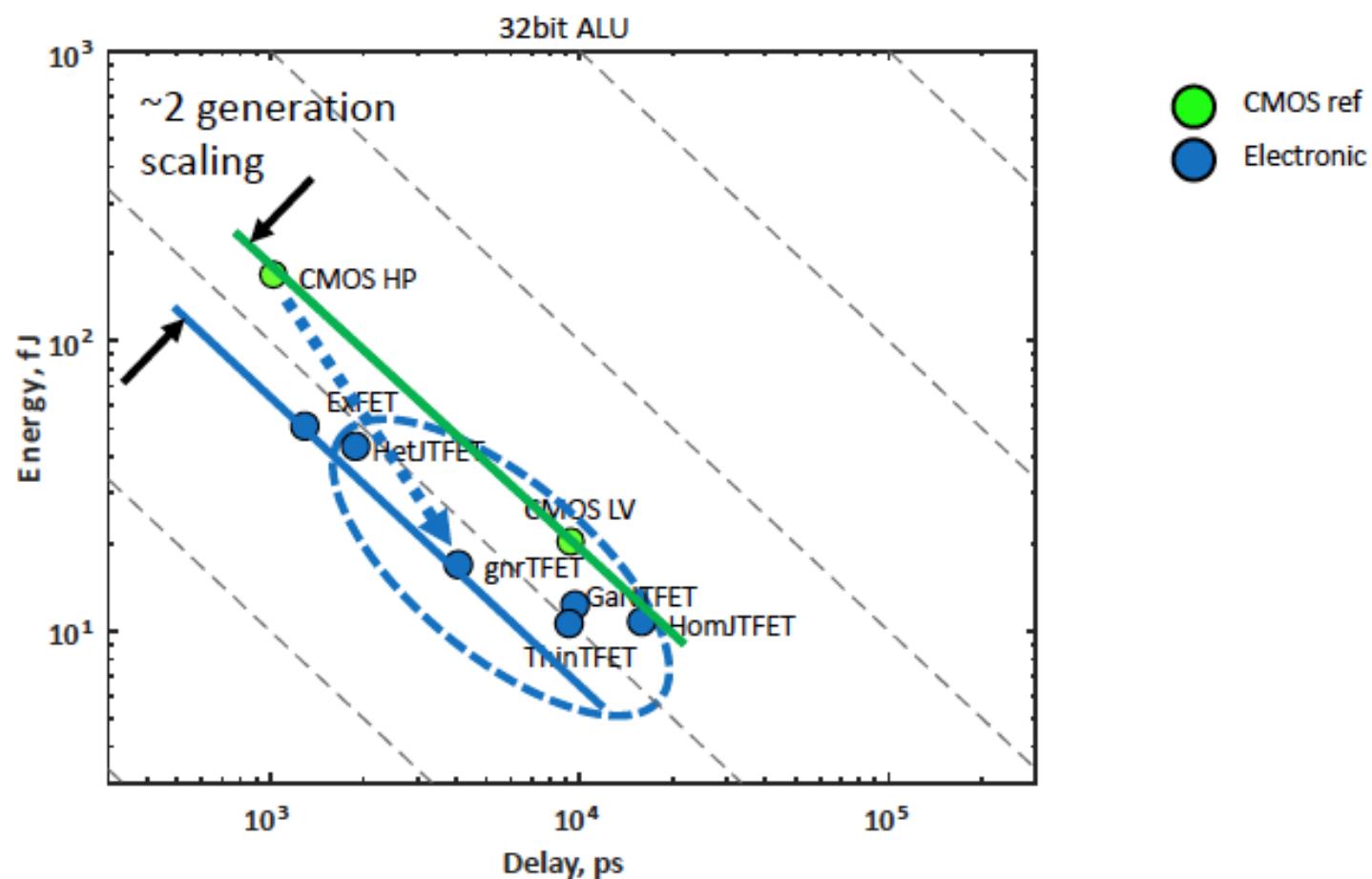


The Changing Measure of Improvement



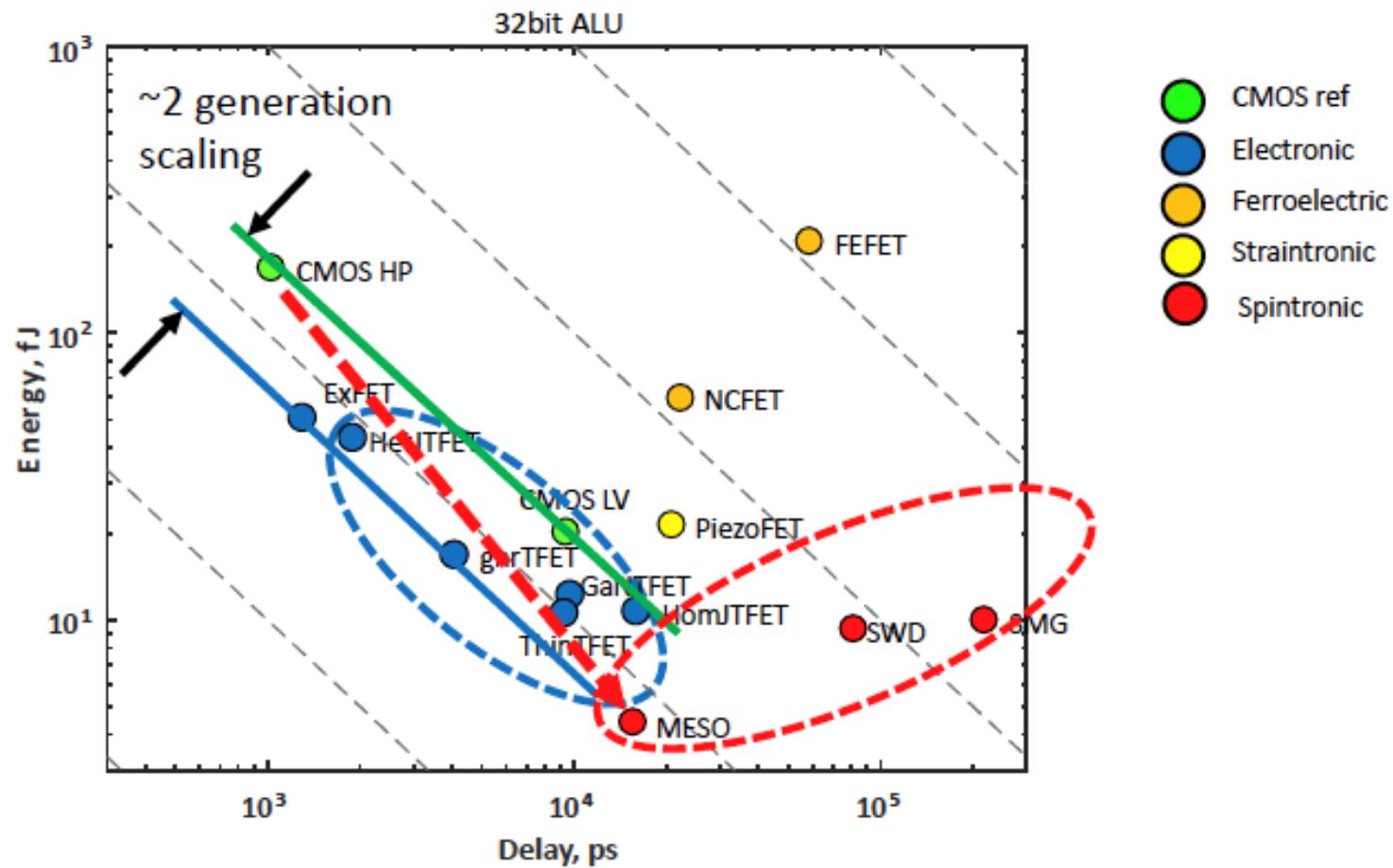
Source: ITRS 2011

The Changing Measure of Improvement



Sources: ITRS 2011, Nikonov and Young, IEEE JxCDC, 1, 3-11 (2015);
Manipatruni, Nikonov and Young, Arxiv cond-mat 1512.05428 (2015)

The Changing Measure of Improvement

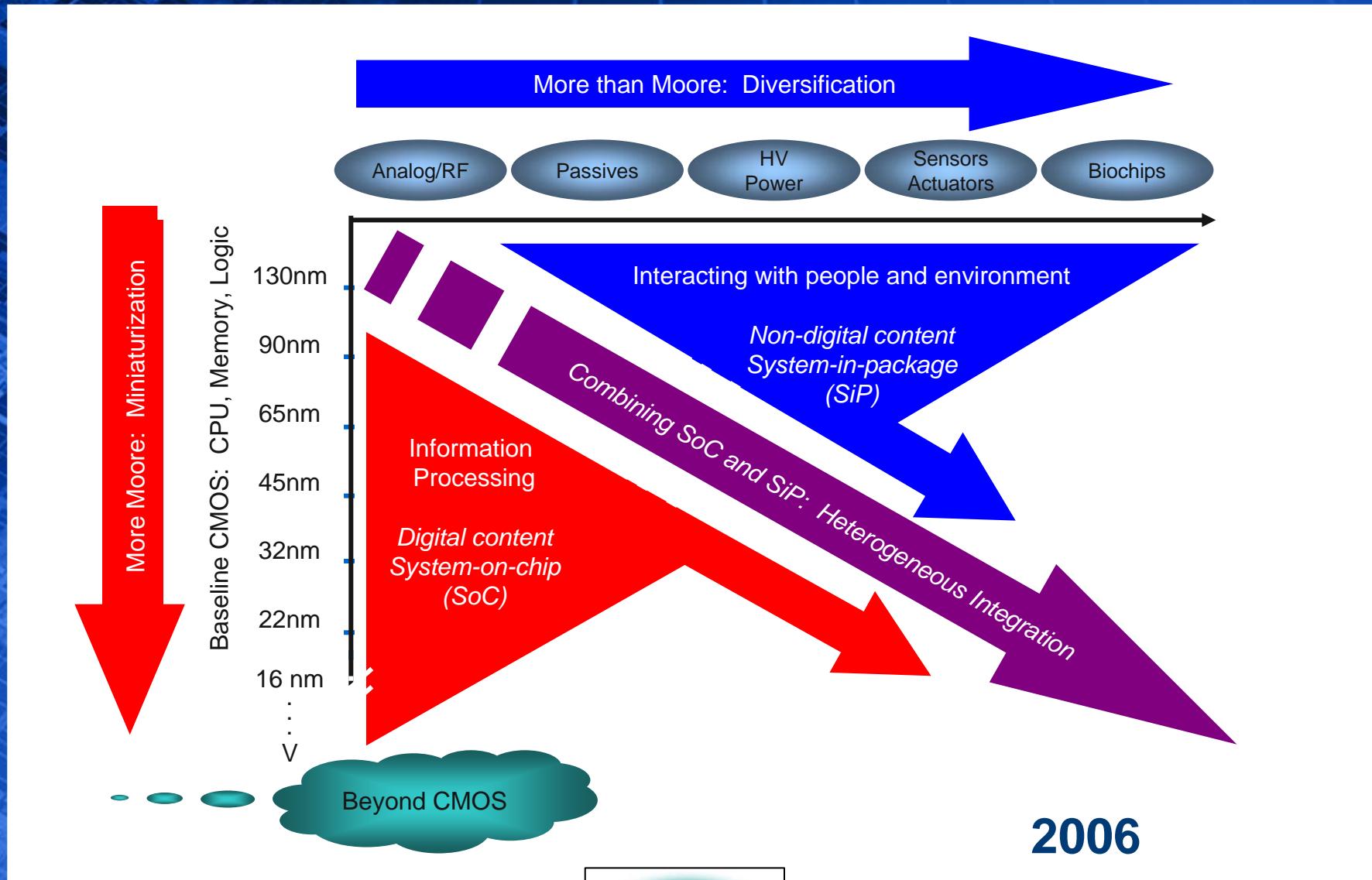


Sources: ITRS 2011, Nikonov and Young, IEEE JxCDC, 1, 3-11 (2015);
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MM+MtM=Heterogeneous Integration



iPhone

June 2007



On January 9, 2007 Steve Jobs announced the iPhone at the Macworld convention, receiving substantial media attention,[16] and that it would be released later that year. On June 29, 2007 the first iPhone was released.

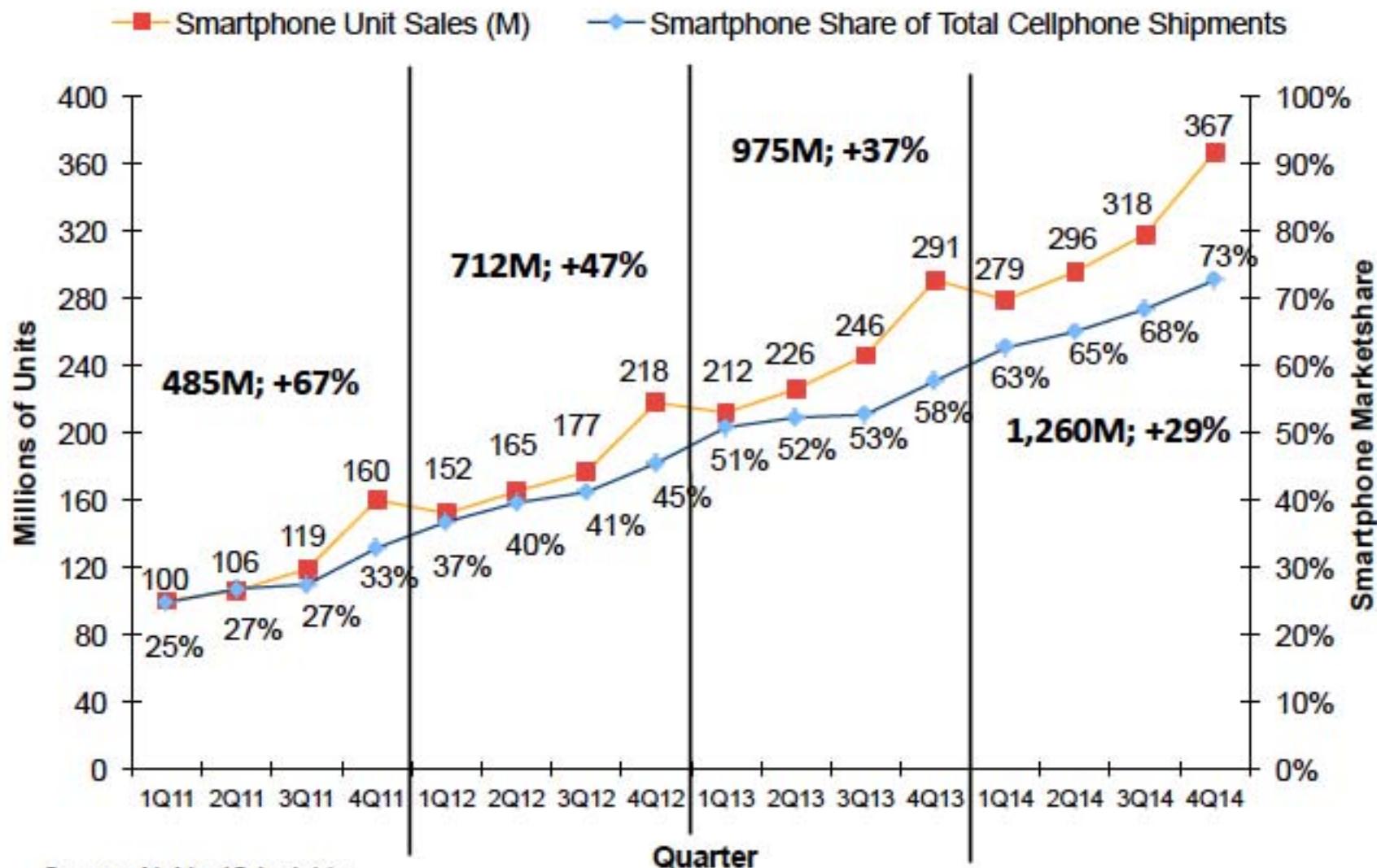
Tablet

April 2010



A WiFi-only model of the tablet was released in April 2010, and a WiFi+3G model was introduced about a month later

Smartphone Marketshare Trends



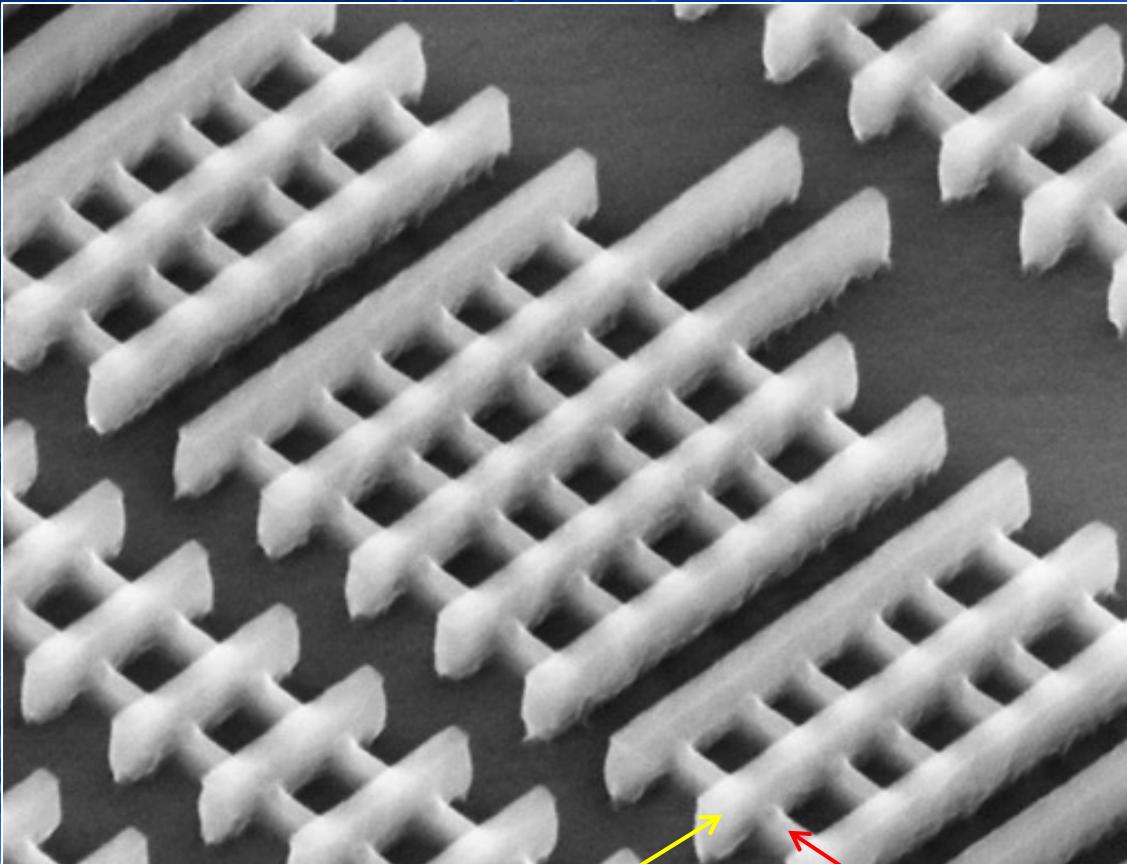
Source: Nokia, IC Insights

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2D → 3D

22 nm Tri-Gate Transistor



Mark Bohr, Kaizad Mistry, May 2011

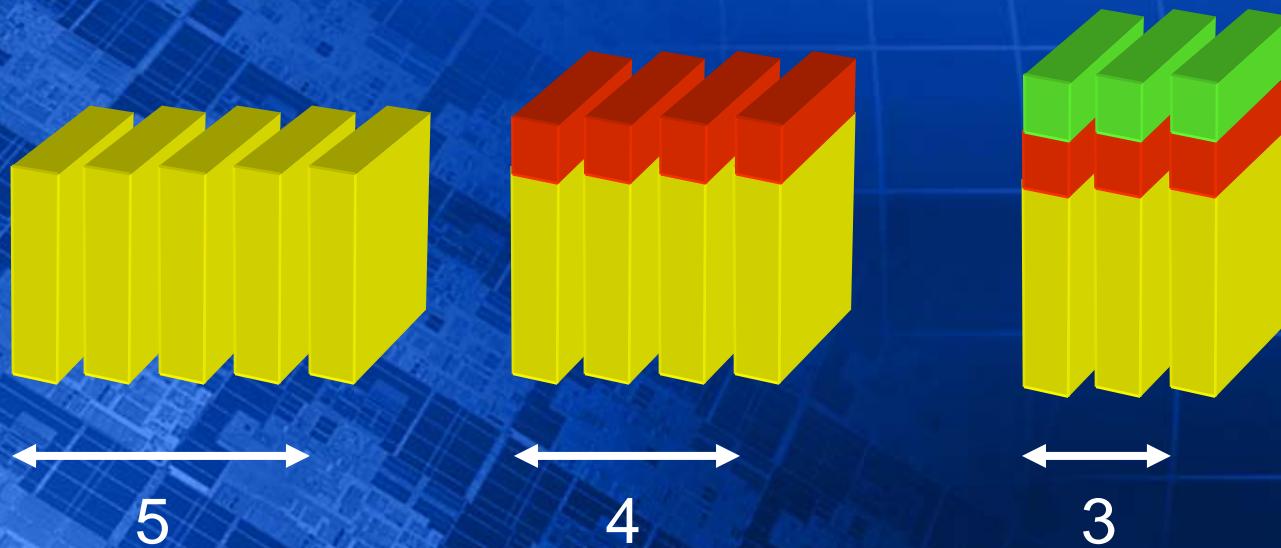
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Question

**How many more technology generations
can
Equivalent Scaling be extended for ?**

Multigate FET Offers a Simple Way for Scaling and Improving Performance

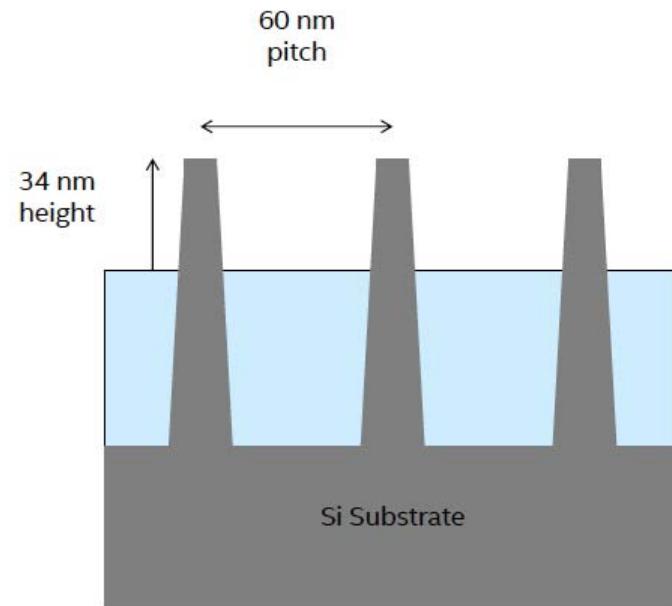


Semicon Japan, December 6, 2013

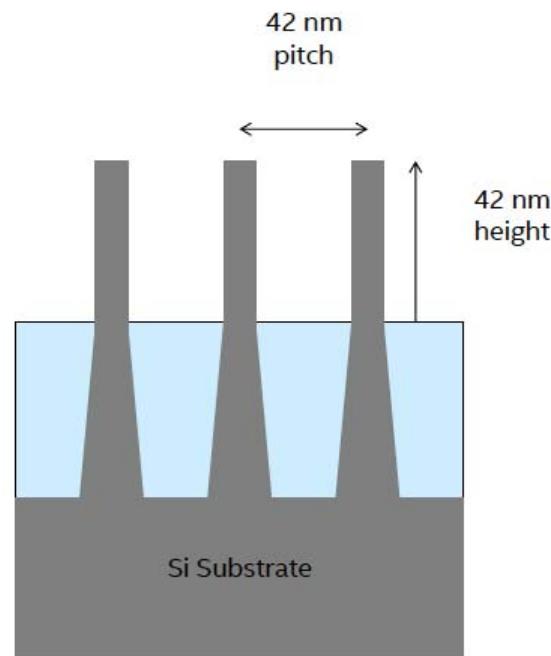
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Transistor Fin Improvement



22 nm Process



14 nm Process

Taller and Thinner Fins for Increased Drive Current and Performance



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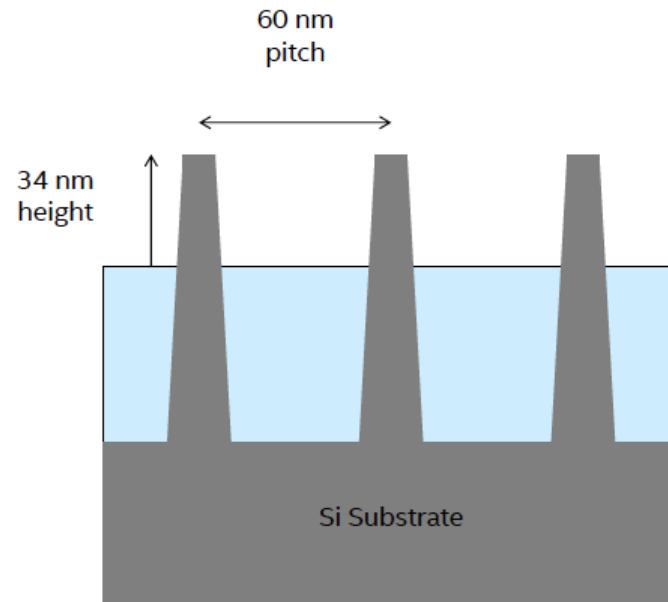
Mark Bohr, August 11, 2014

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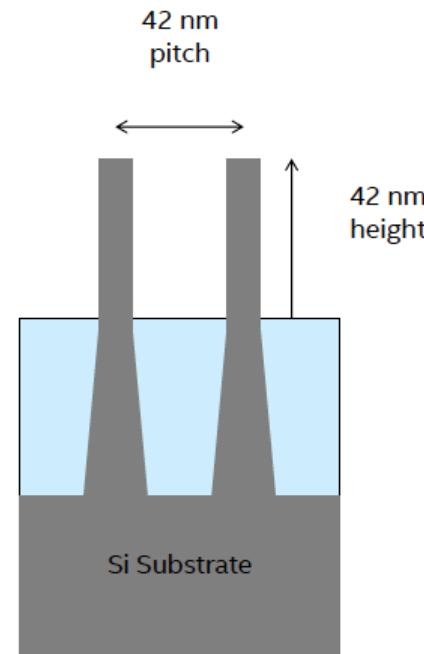
April 2016

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Transistor Fin Improvement



22 nm Process



14 nm Process

*Reduced Number of Fins for Improved Density
and Lower Capacitance*



20

Mark Bohr, August 11, 2014

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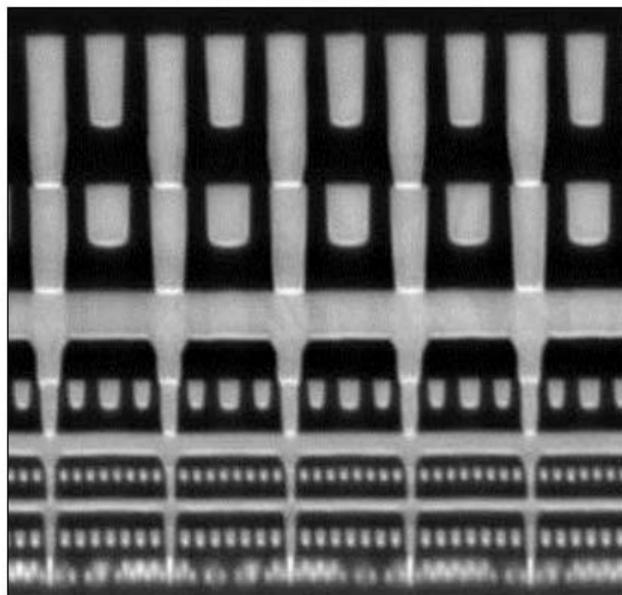
April 2016

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Fin FET Moore's Law Acceleration

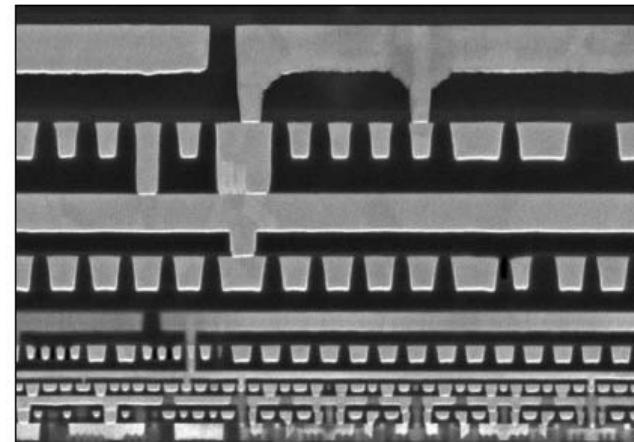
Interconnects

22 nm Process



80 nm minimum pitch

14 nm Process



52 nm (0.65x) minimum pitch

*52 nm Interconnect Pitch Provides
Better-than-normal Interconnect Scaling*



23

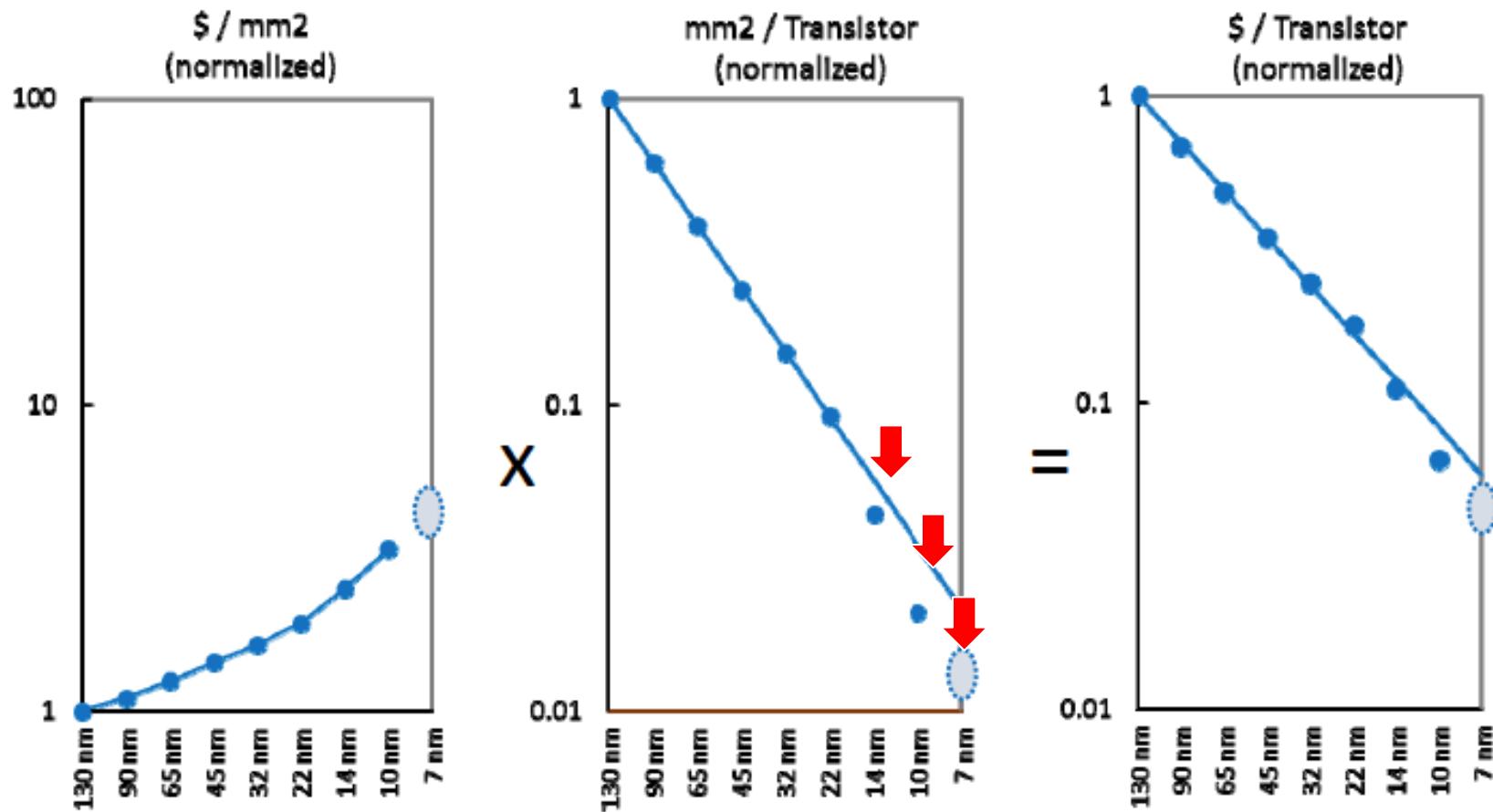
Mark Bohr, August 11, 2014

SPCC

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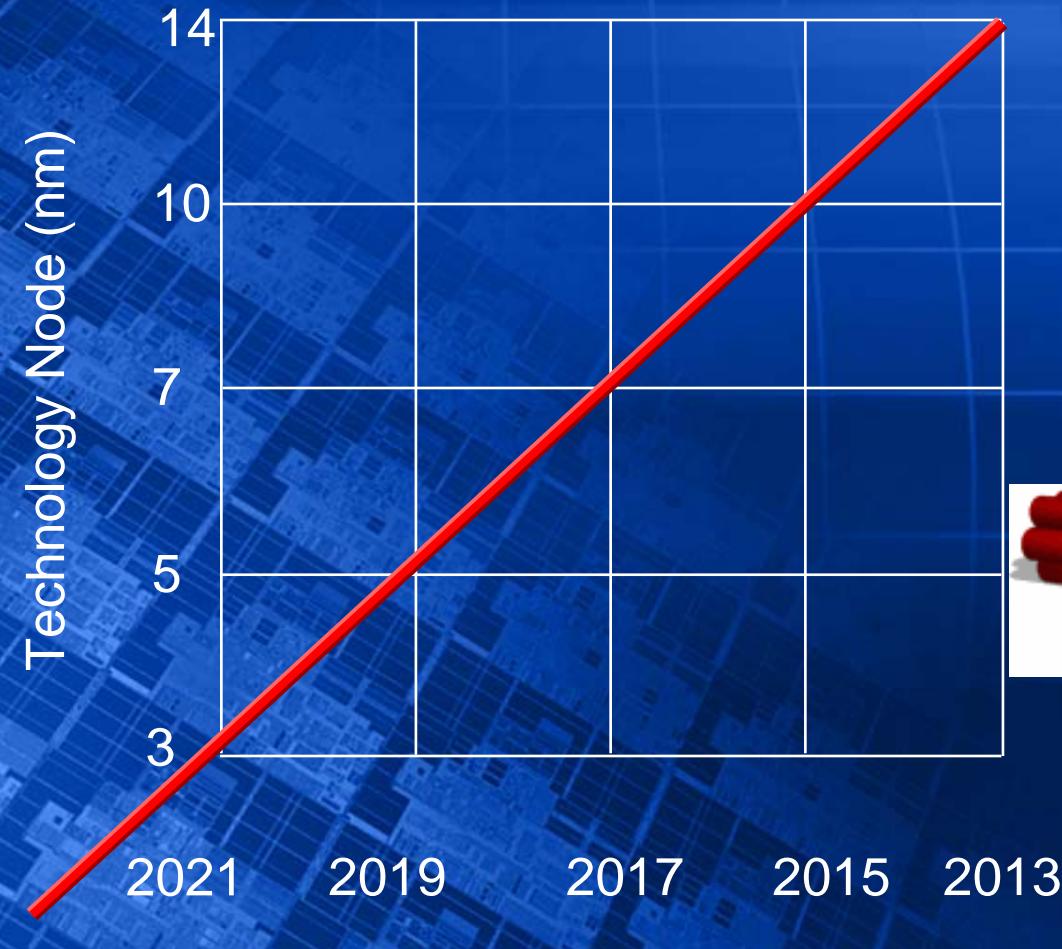
April 2016

Offsetting Wafer Cost with Density



Technology Node Scaling

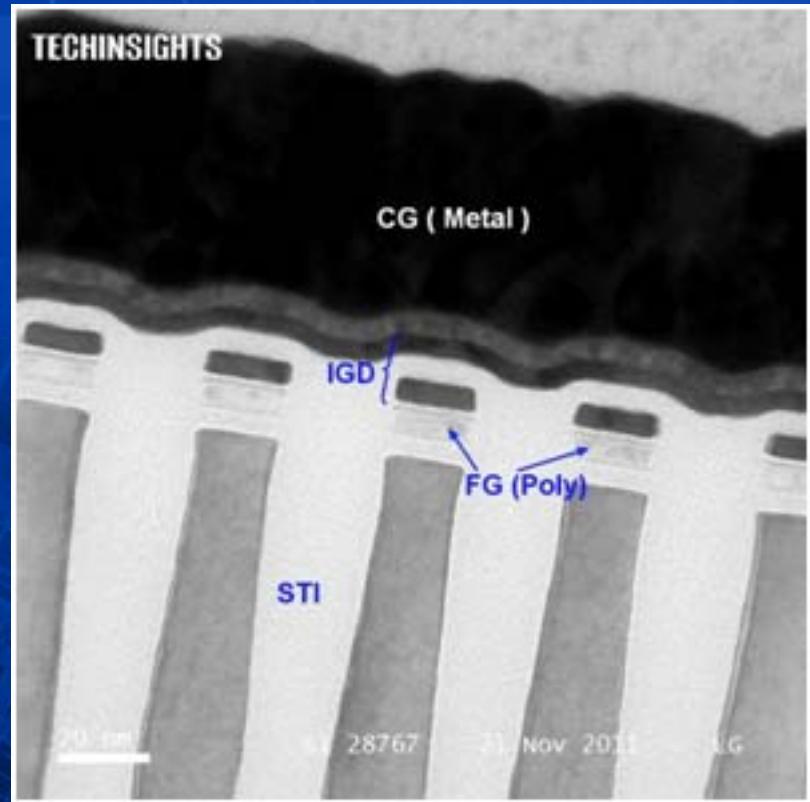
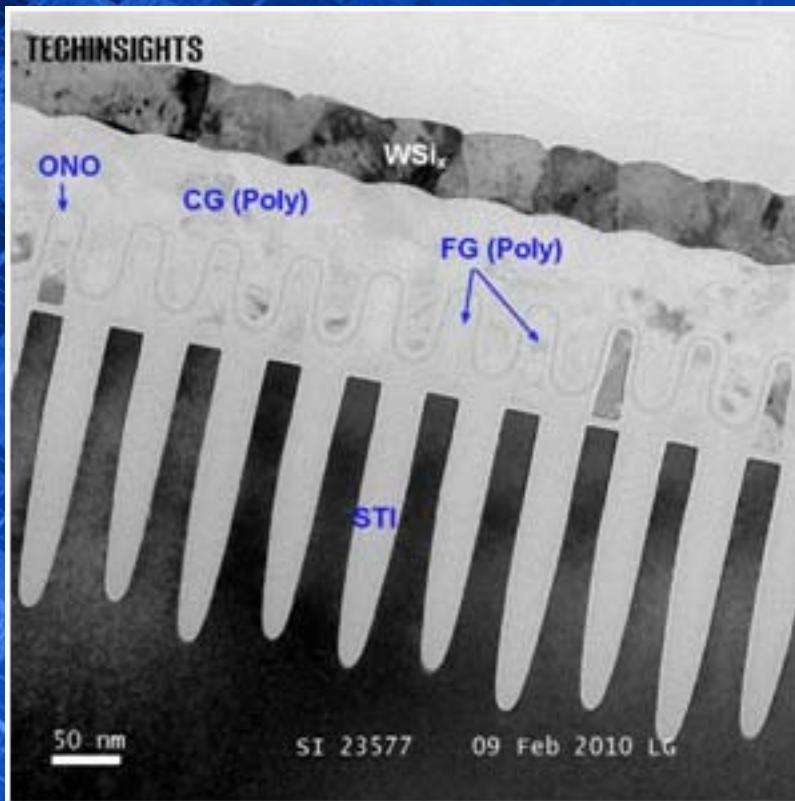
Today's Challenge



2013 ITRS
SPCC



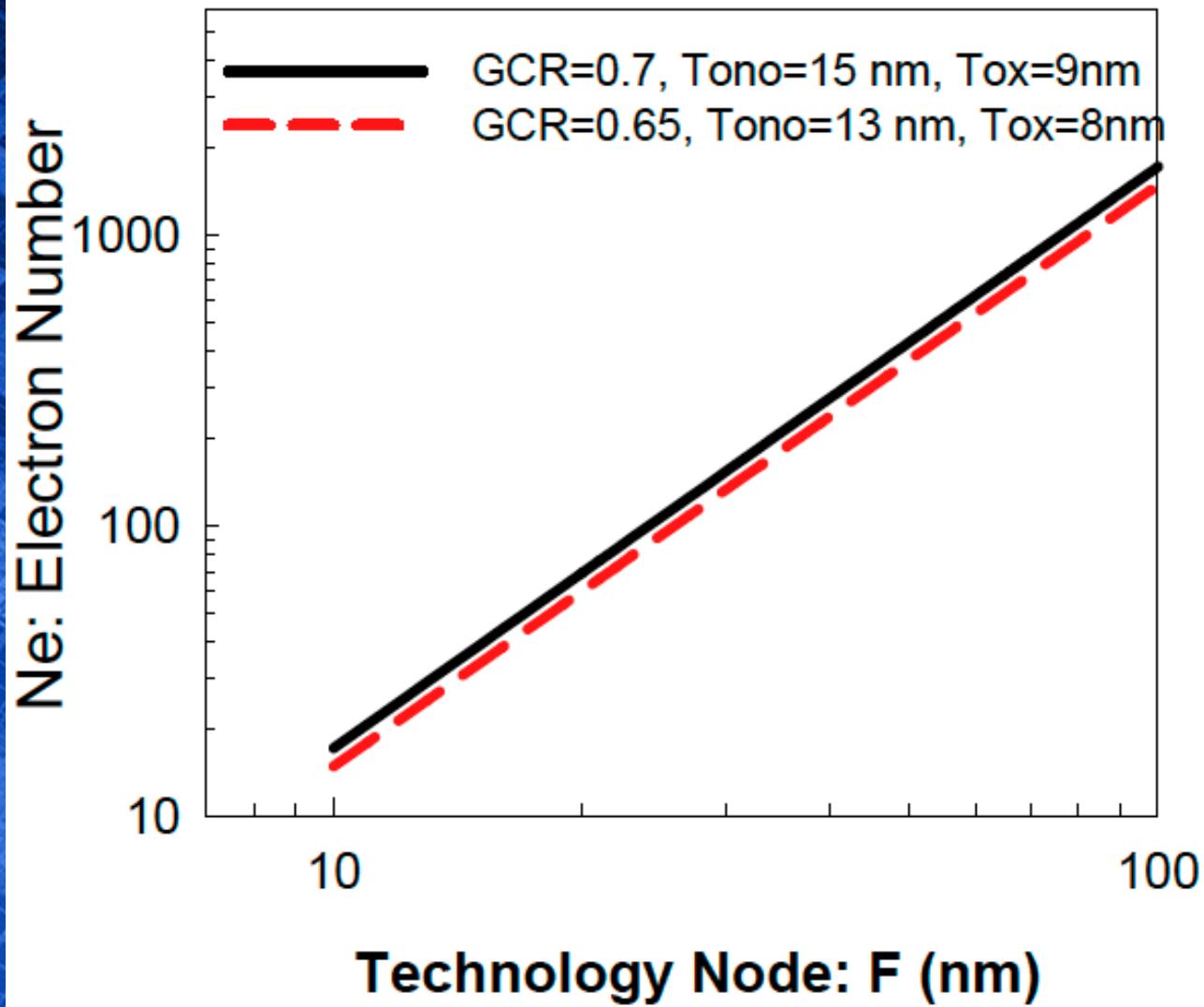
Micron/ Intel 20-nm 64G MLC NAND Flash



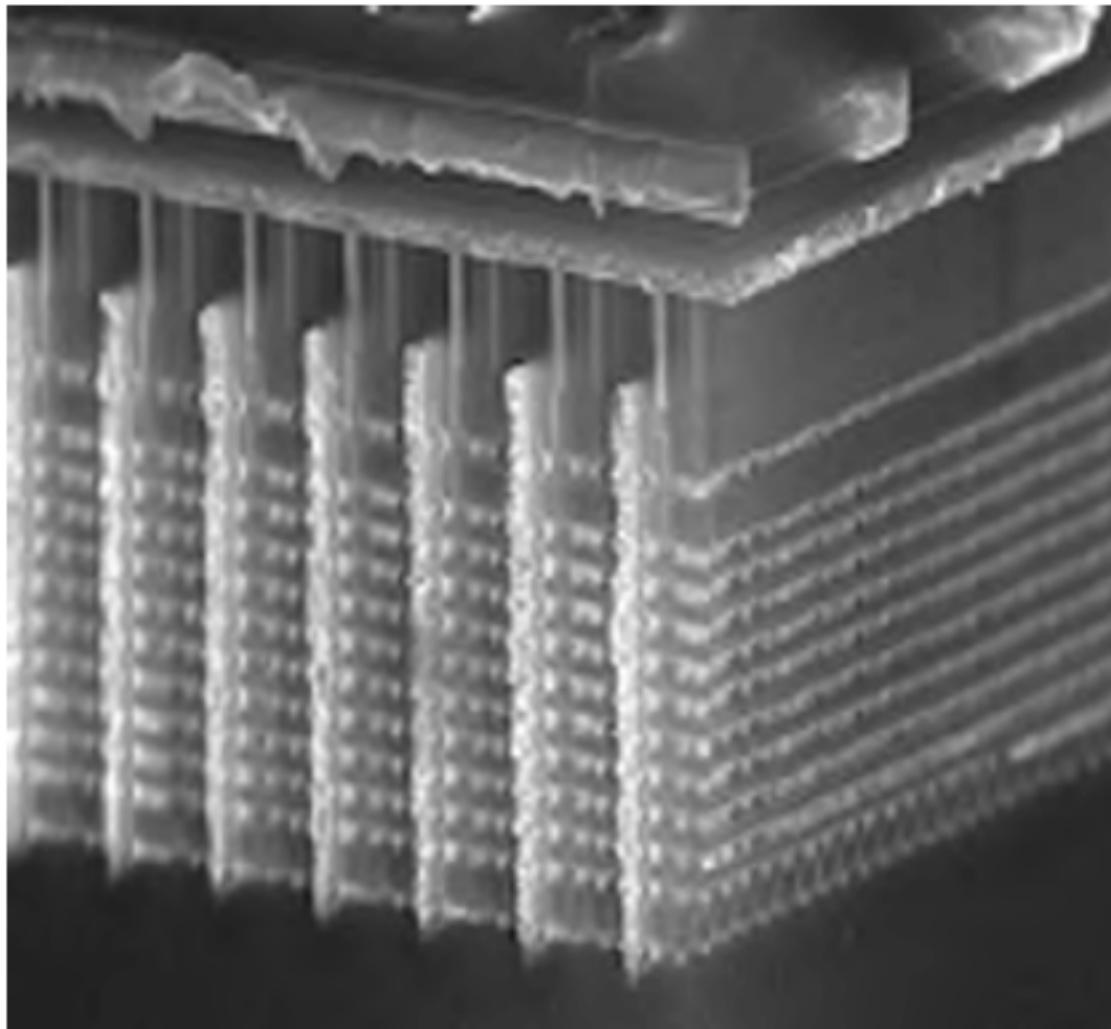
NAND Relative Wafer Cost



Electron number of FG

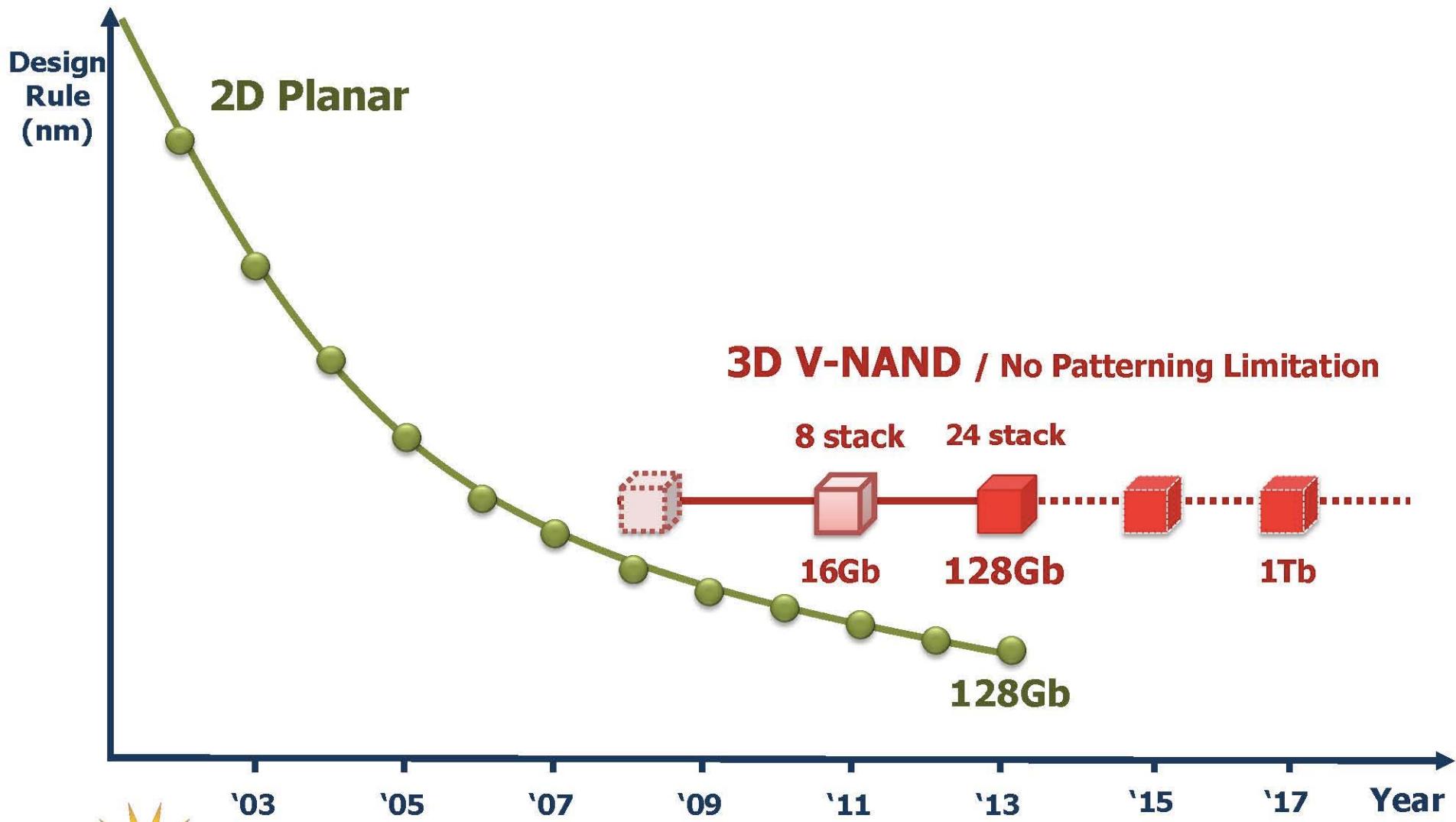


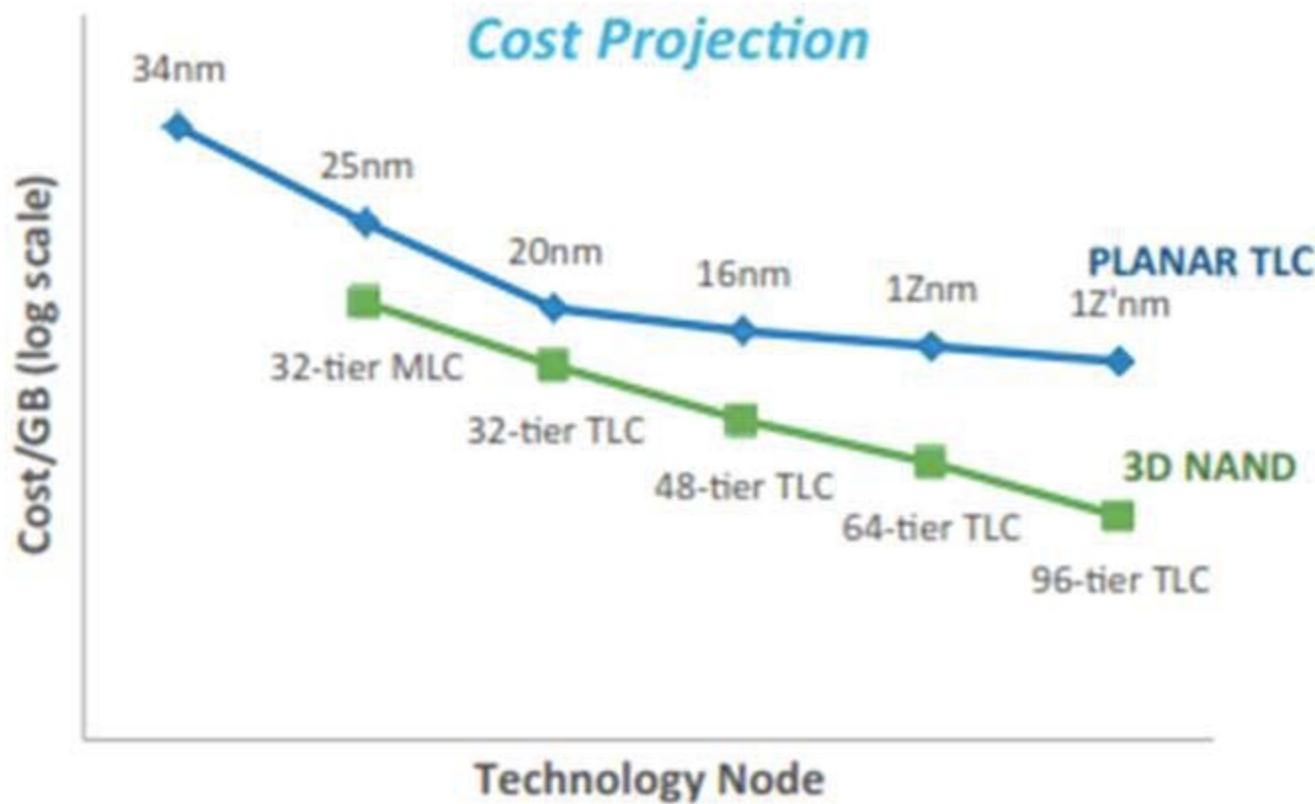
Samsung's 32-Layer 3D V-NAND Memory Chip



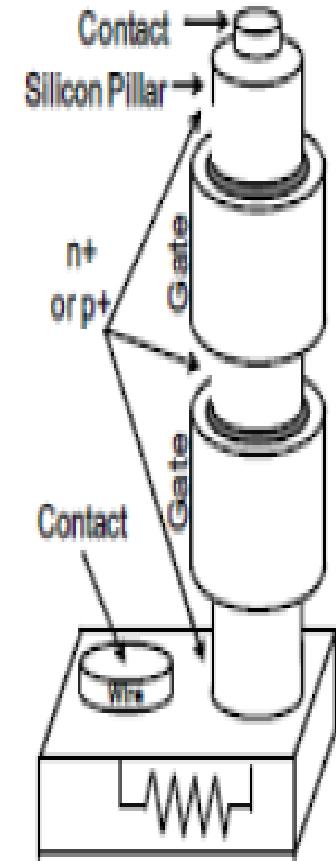
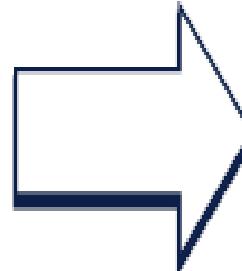
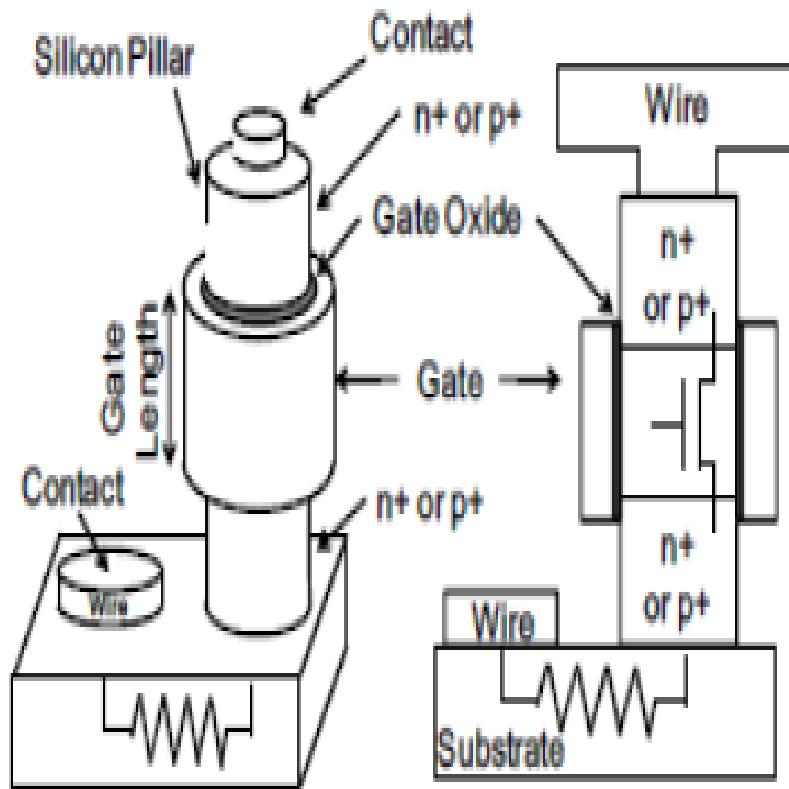
Source: PC Perspective, Samsung

V-NAND Era for the Future



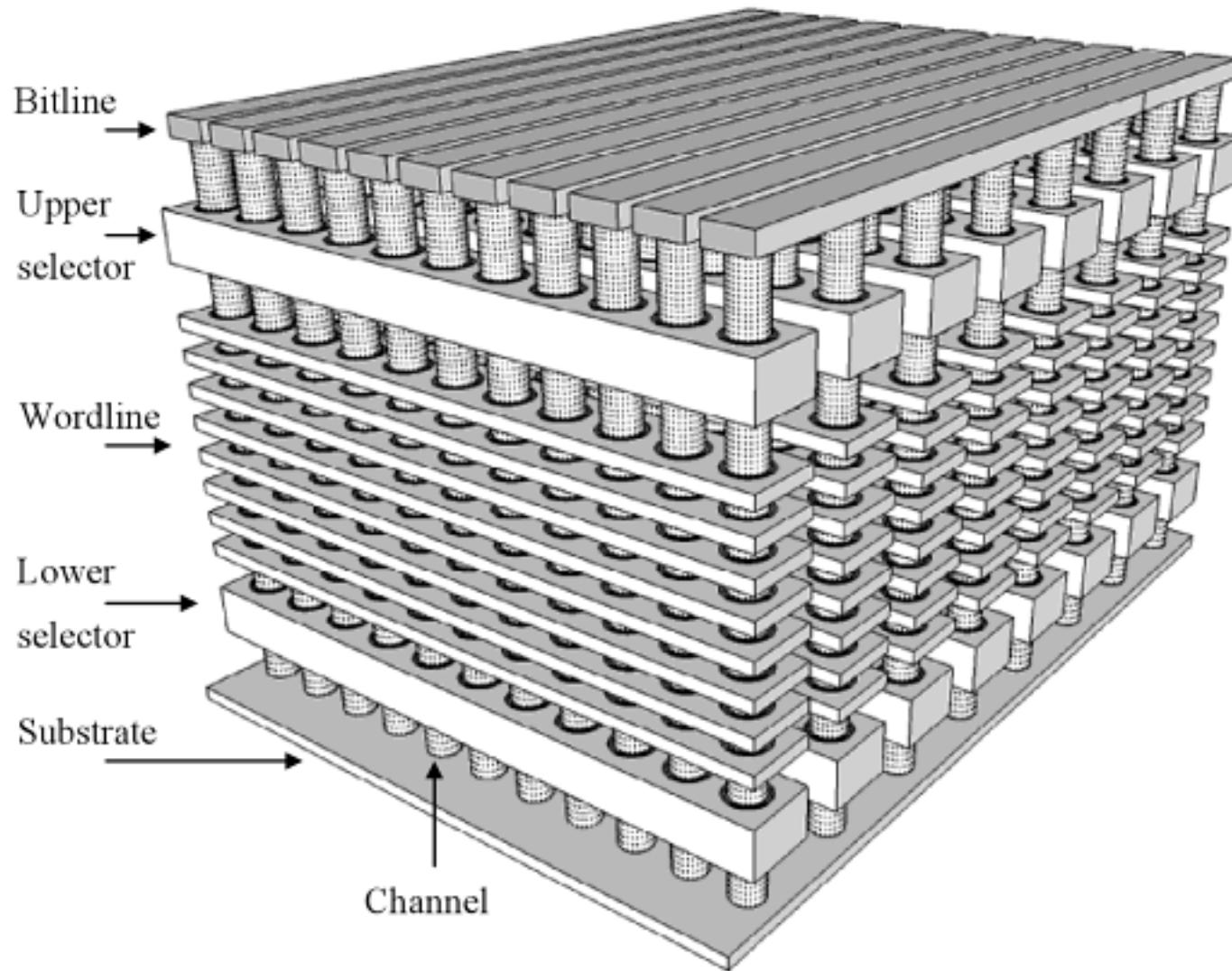


Vertical Logic Architecture



3D Moore's Law Acceleration

3D Architecture



Multiple Stories

1. Introduction
2. 1998. ITRS 1.0
 1. Equivalent Scaling
3. 2000. NNI.
4. 2005. Nanoelectronics Research Initiative (NRI)
5. 2005-6. MPU power limits
6. 2006. More than Moore
 1. Heterogeneous Integration
7. 2010. First Selection of post CMOS devices
8. 2011. Equivalent scaling fully in production
9. 2014. Scaling acceleration
10. **2014-15. ITRS 2.0**
11. **2015. Post CMOS map of devices**
12. 2016. IRDS
13. **2017-2021. 3D POWER Scaling**

Phase 3

Third Age of Scaling (3D Power Scaling)

IC Industry at a Glance (2021->203X)

Driver → Cost/transistor & power reduction

How → 2x Density/2 years (Moore)

Method → 3D Power Scaling (ITRS2.0)

The Different Ages of Scaling

(Different methods for different times)

① Geometrical Scaling (1975-2003)

- ① Reduction of horizontal and vertical physical dimensions in conjunction with improved performance of planar transistors

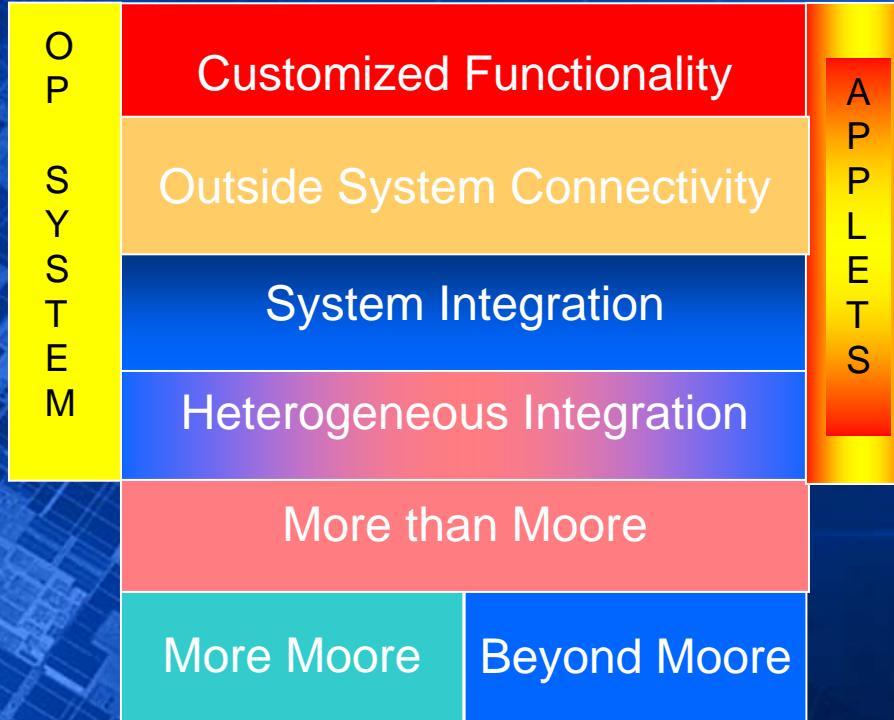
② Equivalent Scaling (2003 ~ 2021)

- ① Reduction of only horizontal dimensions in conjunction with introduction of new materials and new physical effects. New vertical structures replace the planar transistor

③ 3D Power Scaling (2021 ~ 203X)

- ① Transition to complete vertical device structures. Heterogeneous integration in conjunction with reduced power consumption become the technology drivers

Beyond 2020



ITRS 2012



21th Anniversary of TRS

<http://www.itrs2.net>

1991

Micro Tech 2000
Workshop Report

1992NTRS

1994NTRS

1997NTRS

Europe

1998 ITRS
Update

2003 ITRS

2008 ITRS
Update

2013 ITRS

Japan

1999 ITRS

2004 ITRS
Update

2009 ITRS

Korea

2000 ITRS
Update

2005 ITRS

2010 ITRS
Update

Taiwan

2001 ITRS

2006 ITRS
Update

2011 ITRS

USA

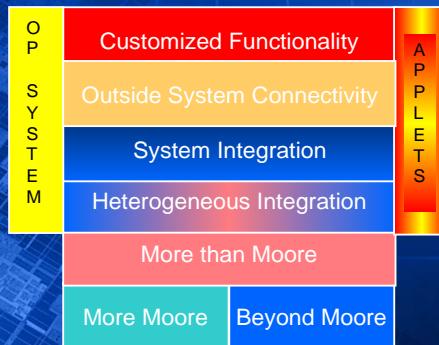
2002 ITRS
Update

2007 ITRS

2012 ITRS
Update

From ITRS to ITRS 2.0

Beyond 2020



Dec 2015



ITRS 2012

P.Gargini

2 Dec 2015

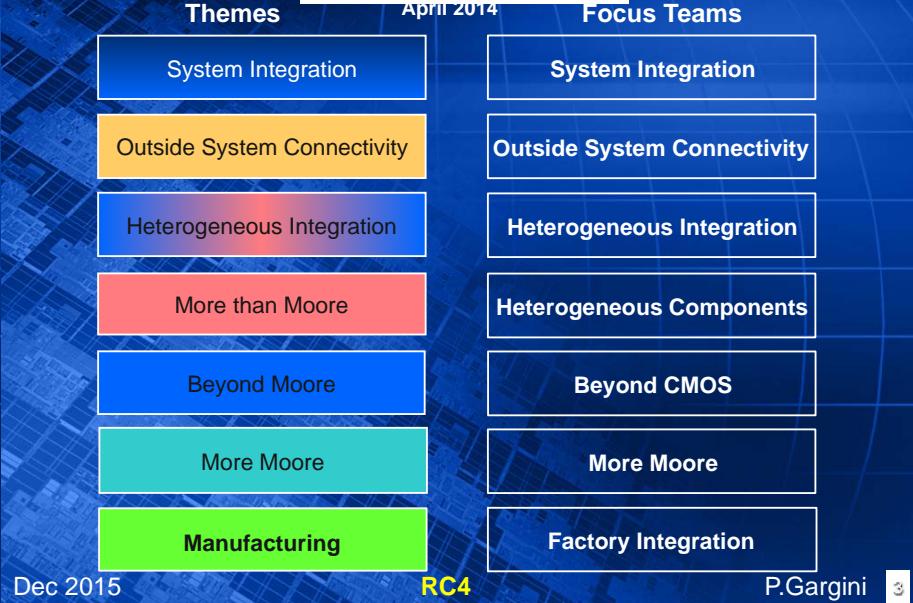
April 2014

SPCC

Beyond 2020

April 2014

Focus Teams



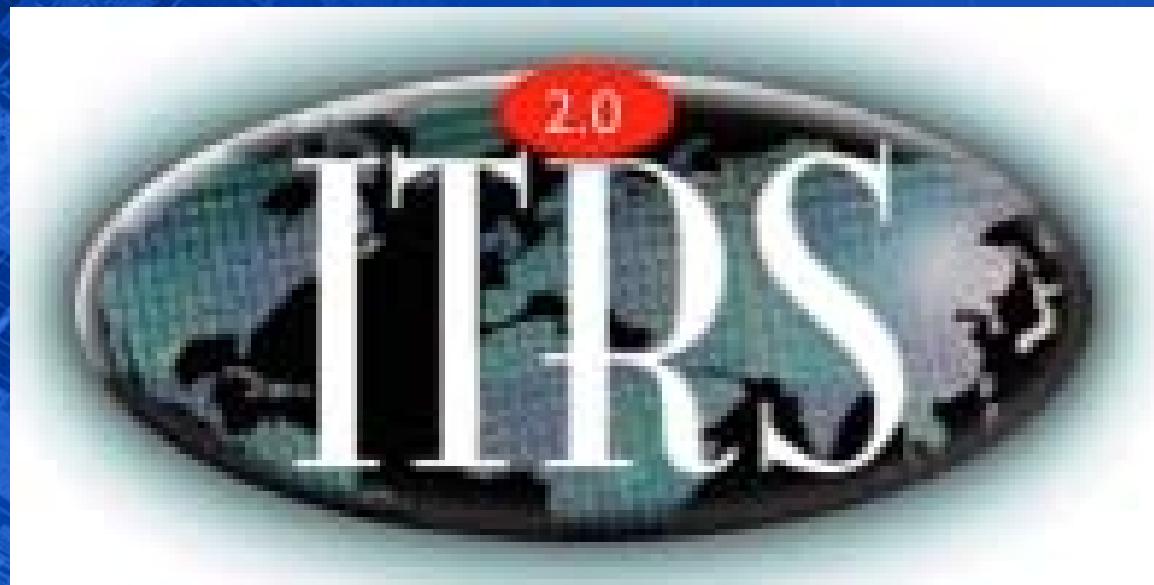
RC4

P.Gargini 3

April 2016

P.Gargini 68

ITRS 2.0



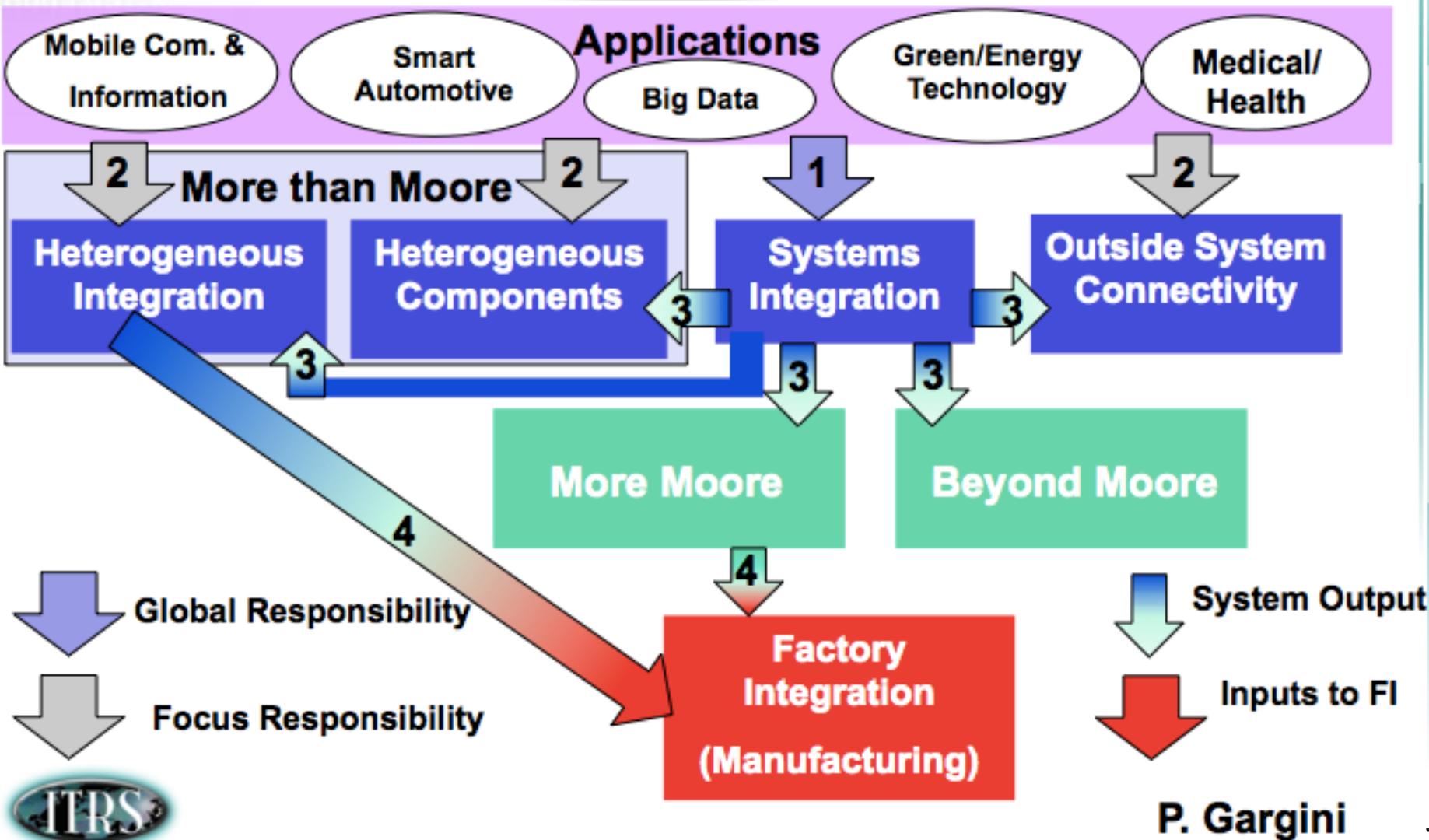
<http://www.itrs2.net>



SPCC

P.Gargini 69

Internet of Things Data Input, Access & Processing Environment



Q: How do we get back to exponential performance scaling?

IEEE Rebooting Computing Initiative





International Technology
Roadmap for Semiconductors

14





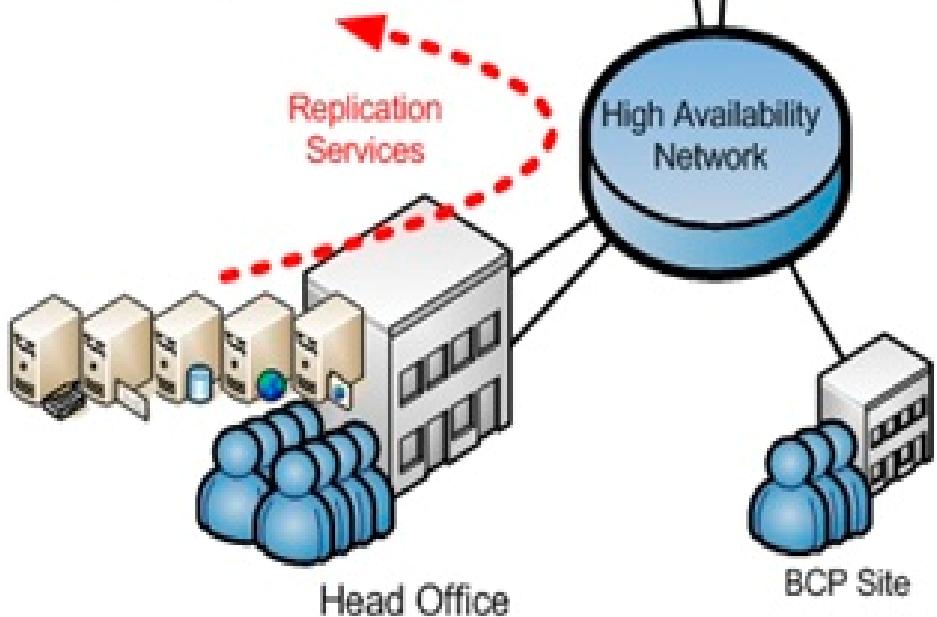
Disaster Recovery
Users

Data Centres

Provisioned Disaster
Recovery Servers



Clustered
Security Appliances



Home Users



Remote Users



Mobile Users

Data Centers

Categories	Year	2015	2017	2019	2021	2023	2025	2027	2029
Data Center Global Indicators	Number of Cores (K)	360	1044	3008	4935	5825	7578	8967	10602
	Total Memory Storage (PB)	300	1559	4676	14029	42088	126264	378792	1136377
	Area of One Server Building (MSF)	0.5	0.9	1.6	2.2	2.2	2.42	2.42	2.42
	Total Power Consumed by Datacenter (MkWh)	779.8	839	1004.7	1137.2	1166.1	1380.7	1635.6	2044.3
	Total Switching Capability of Datacenter BW (Tb/s)	1000	2512	6309	10700	15849	21119	39811	63096
	Data Center Efficiency (GFLOPS/W)	2.4	4.9	10	17	24	33.9	47.9	67.8
Servers	Server Units/Rack	40	40	40	40	40	40	40	40
	Number of Cores/socket	18	29	47	59	74	93	117	147
	Power /Single Server Unit (W)	700	700	700	700	700	700	700	700
	Main Memory / Single Server Unit (GB)	32	45	64	76	91	108	129	154
	Power Consumed by Cores/single socket (W)	165	199	247	294	349	415	441	433
Switching	Network Bandwidth/Unit (Gb/s)	40	40	100	100	100	400	400	400
	Network Bandwidth/Rack (Gb/s)	1600	1600	4000	4000	4000	16000	16000	16000
	Rack Switch Capacity BW (Gb/s)	1200	1200	3000	3000	3000	12000	12000	12000
Power	Power efficiency (Grid delivery/Data Center Use)	0.55	0.57	0.59	0.61	0.63	0.65	0.67	0.69
	Power Consumed by Networking and Switching (MkWh)	21.91	55.05	138.26	87.66	138.93	220.19	348.97	553.08
	Power Consumed by Storage (MkWh)	0.0657	0.259	0.449	0.778	1.347	2.334	4.043	7.004
	Power Consumed for facility cooling (MkWh)	38.99	55.02	86.13	237.31	264.26	307.03	374.89	482.56



Mobile

	Year	2015	2017	2019	2021	2023	2025	2027	2029
Input Metrics	Number of AP cores	4	4	6	8	10	12	14	18
	Number of GPU cores	14	22	34	54	86	138	220	352
	Max frequency of any Component in System (GHz)	2.7	2.9	3.2	3.4	3.7	4	4.3	4.7
	Number of Mega pixels in Display	2.1	2.1	3.7	8.8	8.8	33.2	33.2	33.2
	Band Width between AP and Main memory (Gb/s)	45.3	45.3	64	99.6	89.6	148.2	148.2	148.2
	Number of Sensors	14	16	21	20	21	21	22	22
	Number of Antennas	11	13	13	14	15	15	15	15
	Number of ICs	7-10	7-10	7-10	7-10	7-10	7-10	7-10	7-10
	Cellular data rate growing ~1.3x/year (MB/s)	17.5	12.5	21.63	40.75	40.75	40.75	40.75	40.75
	Wi-Fi data rate evolving with standards (Mb/s)	867	867	867	7000	7000	28000	28000	28000
Output Metrics	PCB area of main Components (cm ²)	62	69	76	84	93	103	103	103
	Board power averaged at ~7%/year (mW)	4274	4706	5183	5708	6287	6926	7630	8406

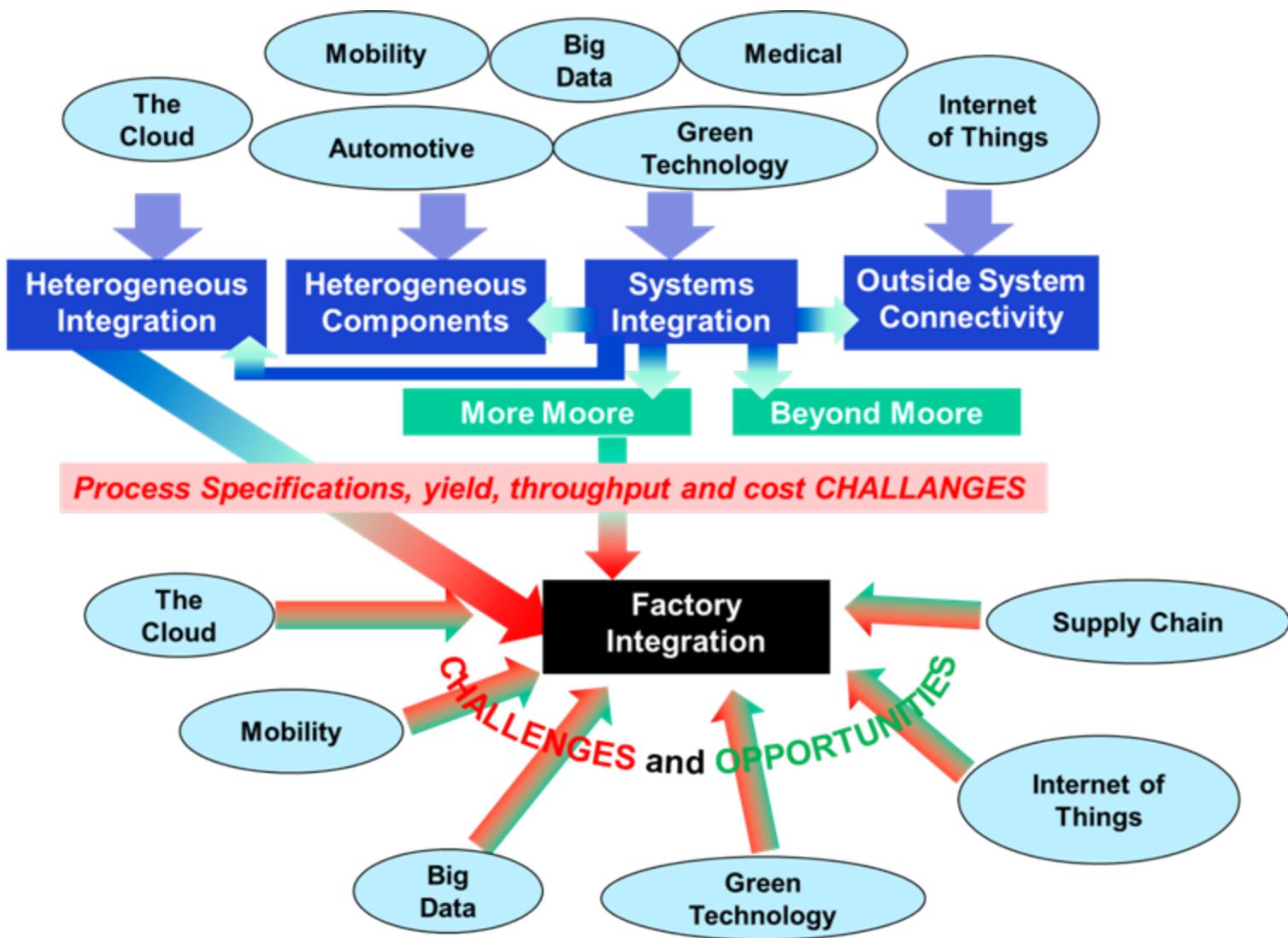
NAND Flash

<i>Year of Production</i>	2015	2016	2020	2022	2024	2028	2030
2D NAND Flash uncontacted poly 1/2 pitch – F (nm)	15	14	12	11	12	12	12
3D NAND minimum array 1/2 pitch - F(nm)	80nm						
Number of word lines in one 3D NAND string	32	32-48	64-96	128	128-192	256-384	384-512
Dominant Cell type (FG, CT, 3D, etc.)	FG/CT/3D						
Product highest density (2D or 3D)	256G	384G	648G	1T	1.5T	3T	4T
3D NAND number of memory layers	32	32-48	64-96	96-128	128-192	256-384	384-512
Maximum number of bits per cell for 2D NAND	3	3	3	3	3	3	3
Maximum number of bits per cell for 3D NAND	3	3	3	3	3	3	3

DRAM TECHNOLOGY	YEAR OF PRODUCTION	2015	2017	2019	2021	2024	2027	2030
Half Pitch (Calculated Half pitch) (nm)	24	20	17	14	12	8.4	7.7	
DRAM cell size (μm^2)	0.00346	0.00240	0.00116	0.00073	0.00048	0.00028	0.00024	
DRAM cell FET structure	RCAT+Fin	RCAT+Fin	VCT	VCT	VCT	VCT	VCT	VCT
Cell Size Factor: a	6	6	4	4	4	4	4	4
Array Area Efficiency	0.55	0.55	0.5	0.5	0.5	0.5	0.5	0.5
V_{int} (support FET voltage) [V]	1.1	1.1	1.1	1.1	0.95	0.95	0.95	0.95
Support min. V_{tn} (25C, $G_{m,max}$, $V_d=55\text{mV}$)	0.40	0.40	0.40	0.40	0.37	0.37	0.37	0.37
Minimum DRAM retention time (ms)	64	64	64	64	64	64	64	64
DRAM soft error rate (fits)	1000	1000	1000	1000	1000	1000	1000	1000
Gb/Ichip target	8G	8G	16G	16G	32G	32G	32G	



YEAR OF PRODUCTION	2015	2017	2019	2021	2024	2027	2030
Logic device technology naming	P70M56	P48M36	P42M24	P32M20	P24M12G1	P24M12G2	P24M12G3
Logic industry "Node Range" Labeling (nm)	"16/14"	"11/10"	"8/7"	"6/5"	"4/3"	"3/2.5"	"2/1.5"
Logic device structure options	finFET FDSOI	finFET FDSOI	finFET LGAA VGAA	finFET LGAA VGAA	VGAA, M3D	VGAA, M3D	VGAA, M3D
LOGIC DEVICE GROUND RULES							
MPU/SoC Metalx ½ Pitch (nm)[1,2]	28.0	18.0	12.0	10.0	6.0	6.0	6.0
MPU/SoC Metal0/1 ½ Pitch (nm)	28.0	18.0	12.0	10.0	6.0	6.0	6.0
Contacted poly half pitch (nm)	35.0	24.0	20.0	16.0	12.0	12.0	12.0
L_g : Physical Gate Length for HP Logic (nm) [3]	24	18	14	10	10	10	10
L_g : Physical Gate Length for LP Logic (nm)	26	20	16	12	12	12	12
FinFET Fin Half-pitch (new) = 0.75 or 1.0 M0/M1 (nm)	21.0	18.0	12.0				
FinFET Fin Width (nm)	8.0	6.0	4.0				
FinFET Fin Height (nm)	42.0	42.0	42.0				
Footprint drive efficiency - finFET	2.15	2.5	2.5				
Lateral GAA Lateral Half-pitch (nm)			12.0	10.0			
Lateral GAA Vertical Half-pitch (nm)			12.0	9.0			
Lateral GAA Diameter (nm)			6.0	6.0			
Footprint drive efficiency - lateral GAA, 3x NWs stacked			2.4	2.8			
Vertical GAA Lateral Half-pitch (nm)				10.0	6.0	6.0	6.0
Vertical GAA Diameter (nm)				6.0	5.0	5.0	5.0
Footprint drive efficiency - vertical GAA, 3x NWs stacked				2.8	3.9	3.9	3.9
Device effective width - [nm]	92.0	90.0	56.5	56.5	56.5	56.5	56.5
Device lateral half pitch (nm)	21.0	18.0	12.0	10.0	6.0	6.0	6.0
Device width or diameter (nm)	8.0	6.0	6.0	6.0	5.0	5.0	5.0



Conclusions

- “**Geometrical Scaling**” led the IC Industry for 3 decades
 - ITRS 1.0**
 - Cooperative and distributed research and manufacturing methods highlighted by **ITRS** emerged as cost effective means of reducing costs since the mid-90s
 - FCRP, NRI, Sematech, IMEC and Government organizations actively cooperated in **advanced research**
- “**Equivalent Scaling**” saved the Semiconductor Industry since the beginning of the previous decade
 - Preliminary evaluation of post-CMOS candidates published in 2010
- **ITRS 2.0**
- “**3D Power Scaling**” is the next phase of (accelerated) scaling
- Post CMOS devices and emerging architectures are being jointly evaluated->ITRS/IEEE RC->IRDS