

# Emerging Interconnect Technologies

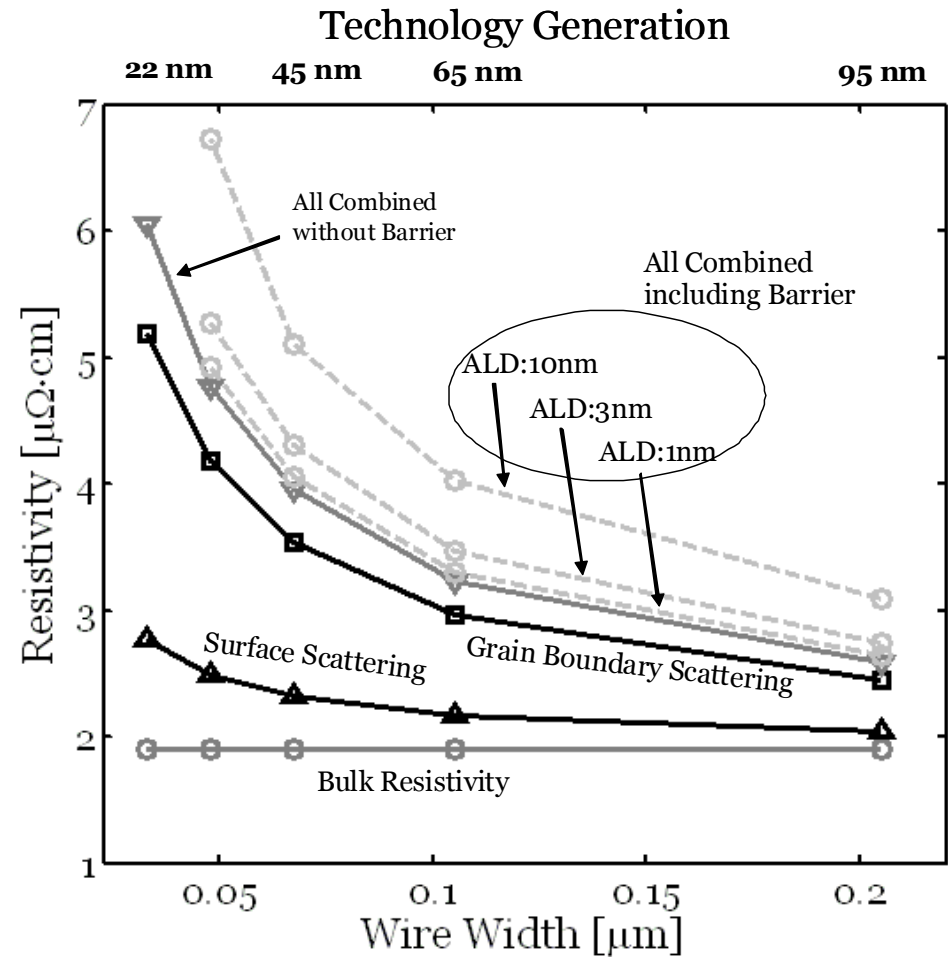
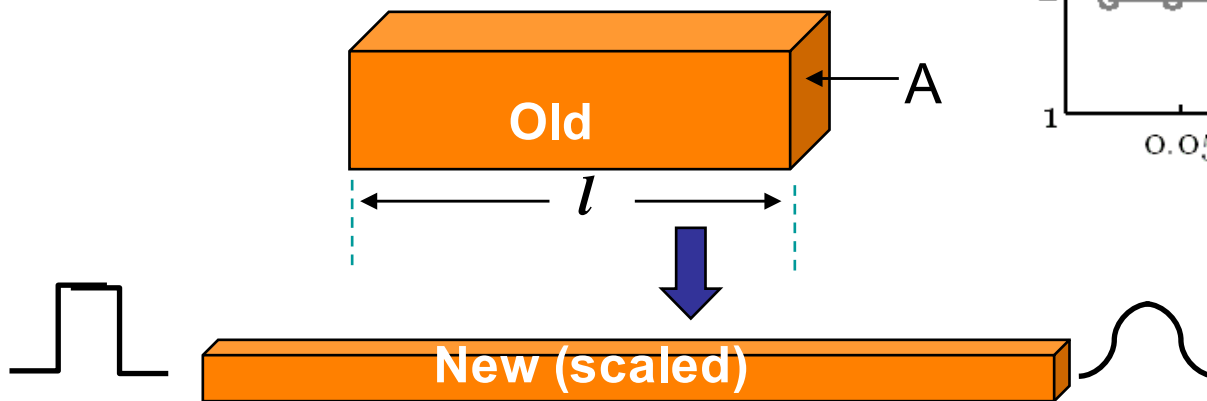
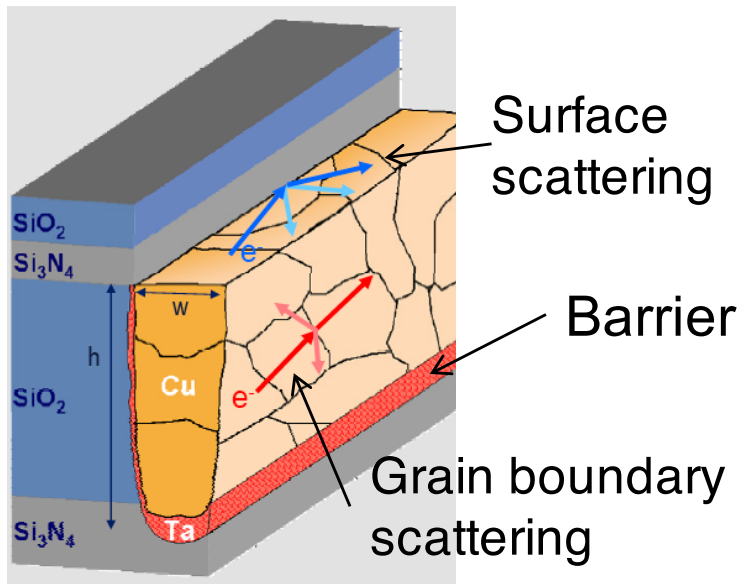
**Prof. Krishna Saraswat**

Department of Electrical Engineering  
Stanford University, Stanford, CA, USA

# Outline

- Scaling limits of interconnects
  - Alternatives to Cu
- Performance simulations
  - Cu, CNT, optical interconnects
- Technology for novel optical interconnects
- 3-D integration
- Summary

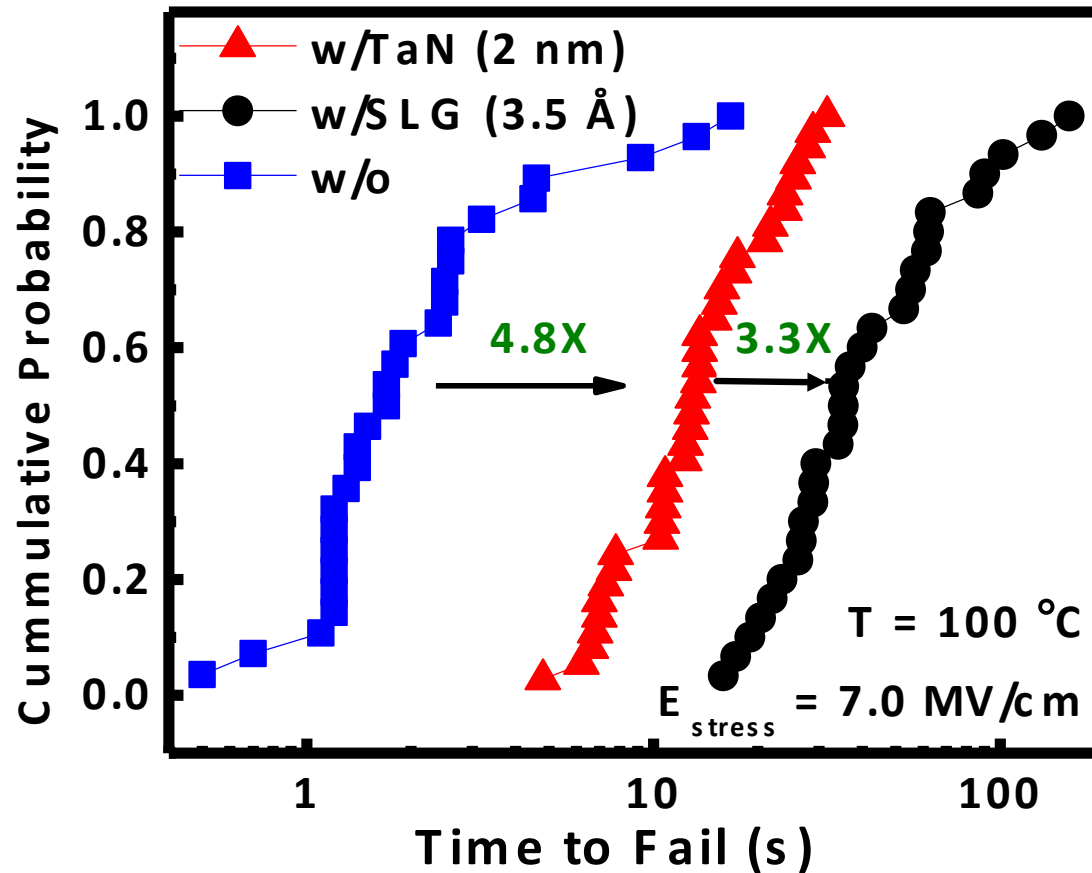
# Effect of Scaling on interconnect performance



$\text{Bit rate} \propto A/l^2$   
 $\text{Delay} \propto l^2/A$   
 $\text{Power dissipation} \sim CV^2f$



# Graphene vs. TaN Barrier for Cu



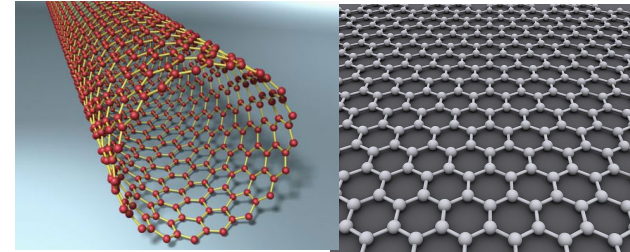
L. Li ... H.-S. P. Wong, *Symp. VLSI Tech.* 2015  
L. Li ... H.-S. P. Wong, *ACS Nano* 2015

**Thinner barrier: 3.5 Å single layer graphene is better than 2 nm TaN**

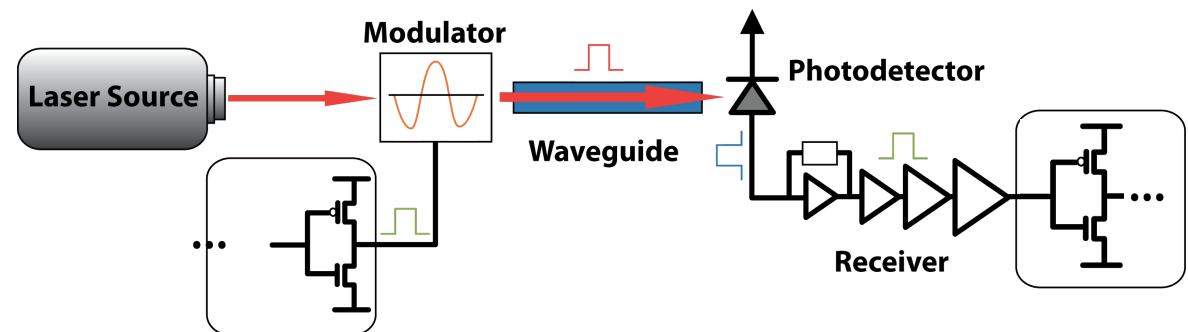


# How can we improve interconnect performance?

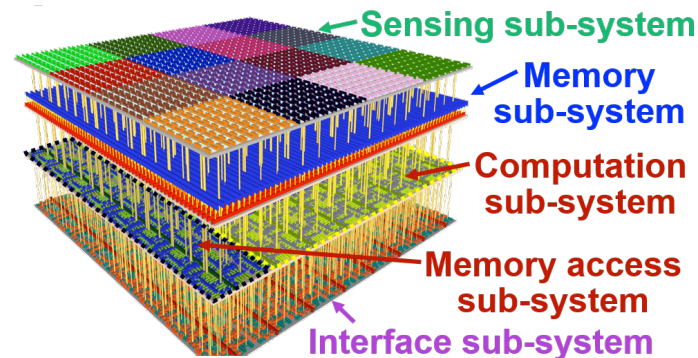
- Carbon nanotubes/ Graphene



- Optical interconnects

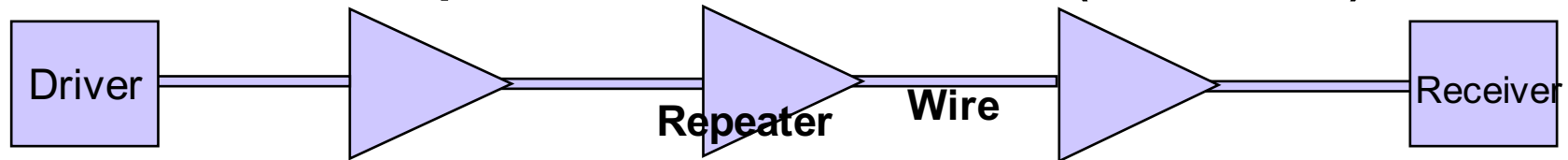


- 3D



# Optical & Electrical Wires: Schematic

## On-chip Electrical Interconnect (Cu or CNT)

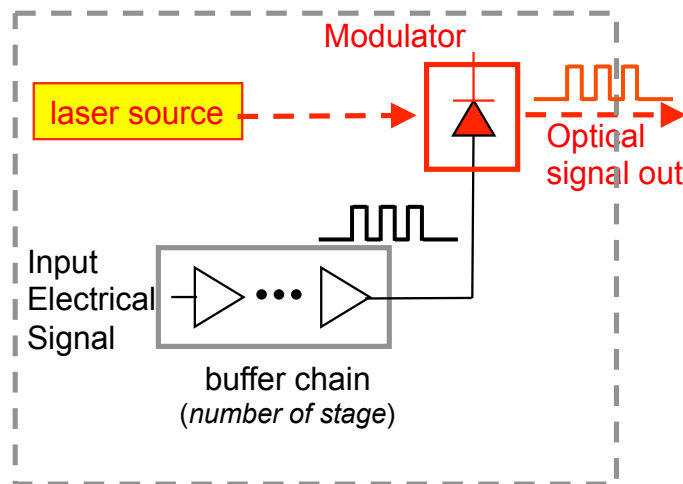


## Off-chip Electrical Interconnect (Cu)



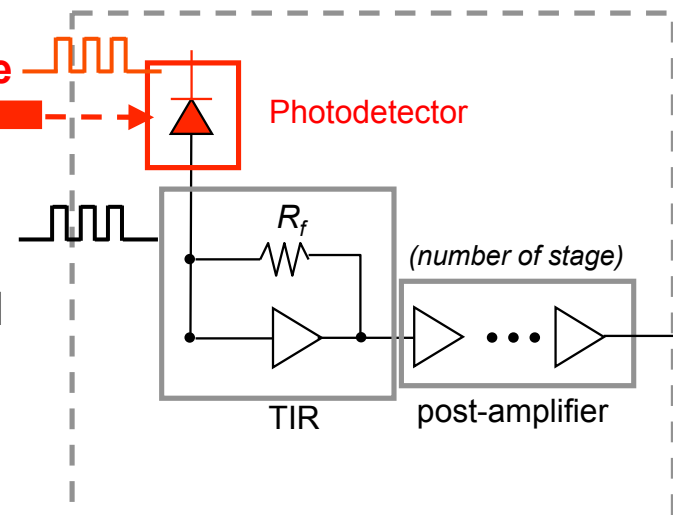
## Optical Interconnect

### Transmitter System



Laser/modulator converts electrical signal into optical signal

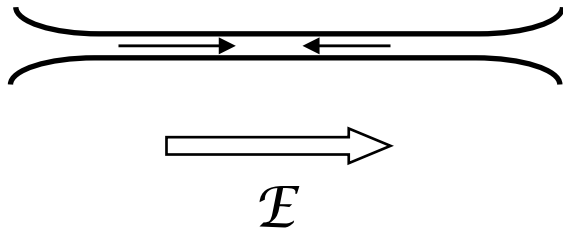
### Receiver System



Photodetector restores optical signal into electrical signal

# Carbon Nanotubes

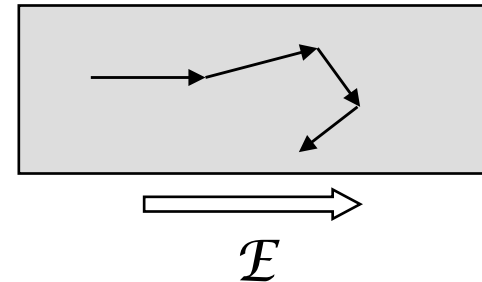
## 1-D conductors:



## Quantum Wires:

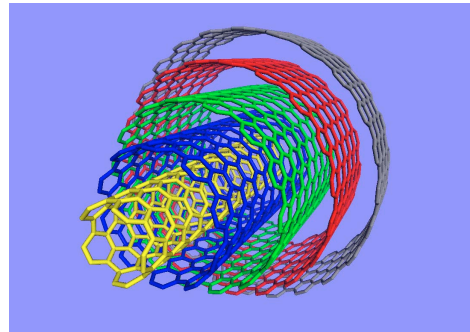
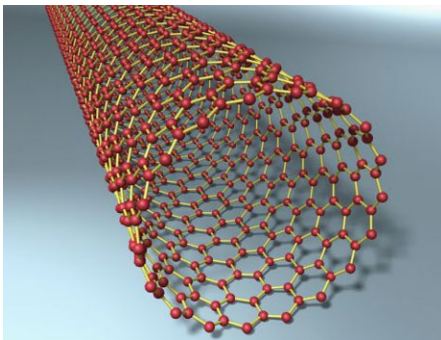
- 1D system with limited density of states. Hence quantum effects play an important role in determining the values of R, L and C
- Mean free paths as large as  $1.6\mu\text{m}$ .

## 3-D conductors:



## Conventional wires :

- Backscattering through a series of small angle scatterings.
- Mean free paths  $\sim 30\text{nm}$ .

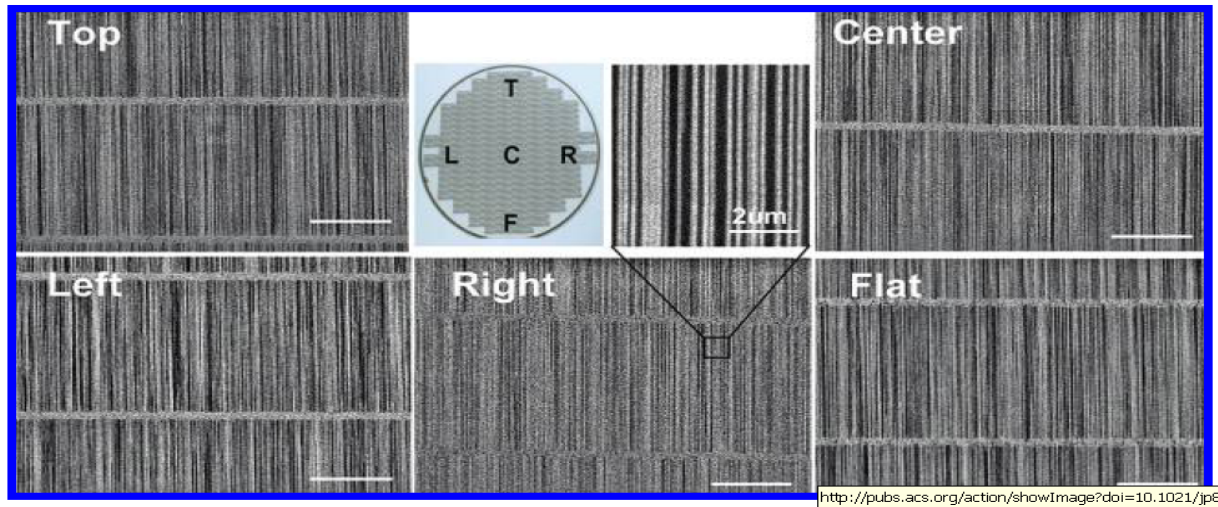


Potential Candidates for  
GSI Interconnects.

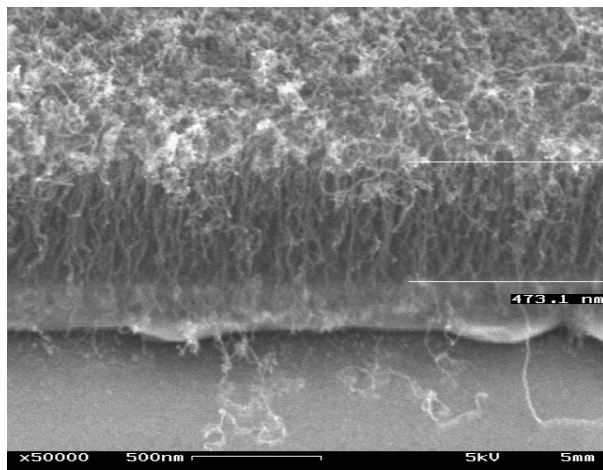
# Formidable Task: Dense Bundles of SWNTs

## Horizontal Growth for Interconnects

Y. Nishi and H.-S. Philip Wong (Stanford)



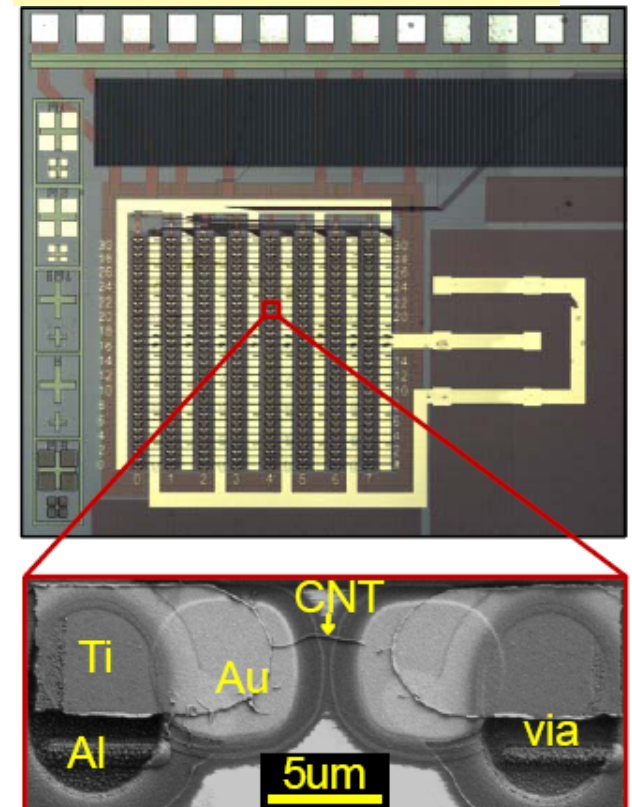
## Vertical Growth



C.V. Thompson, MIT

## 256-Element CNT Ring Oscillator

H.-S. Philip Wong (Stanford)

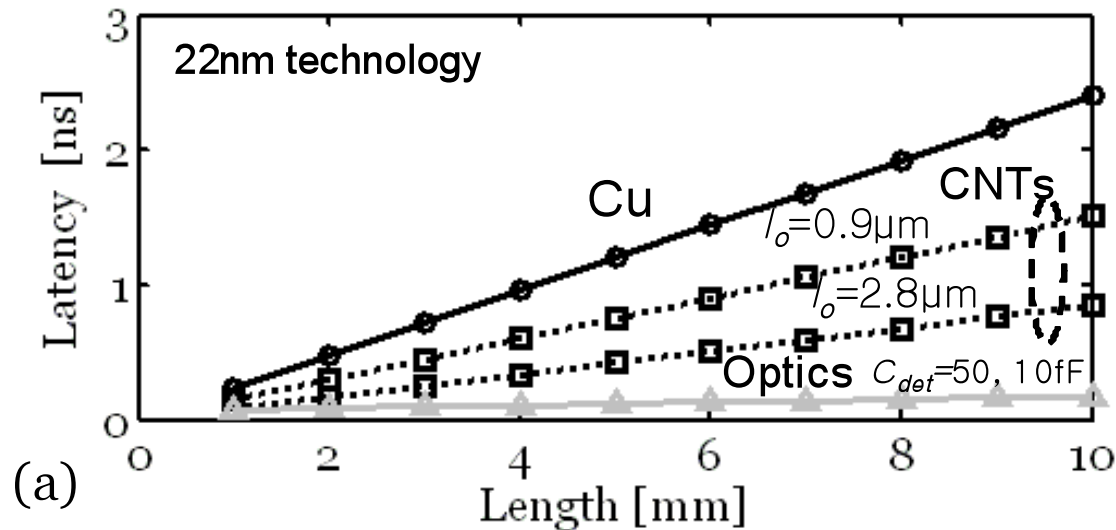


Promising progress in creating aligned isolated SWNTs by transferring **SWNTs grown on sapphire** to other substrates

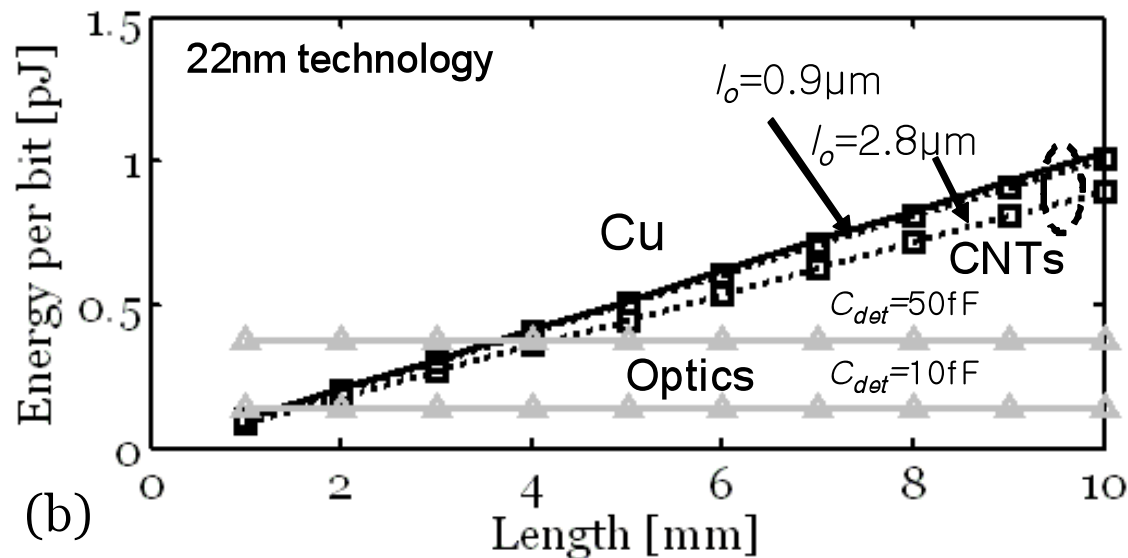
# Potential reliability performance comparison

- **Good thermal conductivity**
  - Graphene:  $4.84 \times 10^3 \sim 5.30 \times 10^3 W / mK$
  - CNT:  $1.75 \times 10^3 \sim 5.80 \times 10^3 W / mK$
  - Copper:  $385 W / mK$
- **High breakdown current**
  - Graphene:  $\sim 10^8 A / cm^2$
  - CNT:  $\sim 10^9 A / cm^2$
  - Copper (EM threshold):  $\sim 10^7 A / cm^2$

# Latency and Energy/bit vs. Wire Length



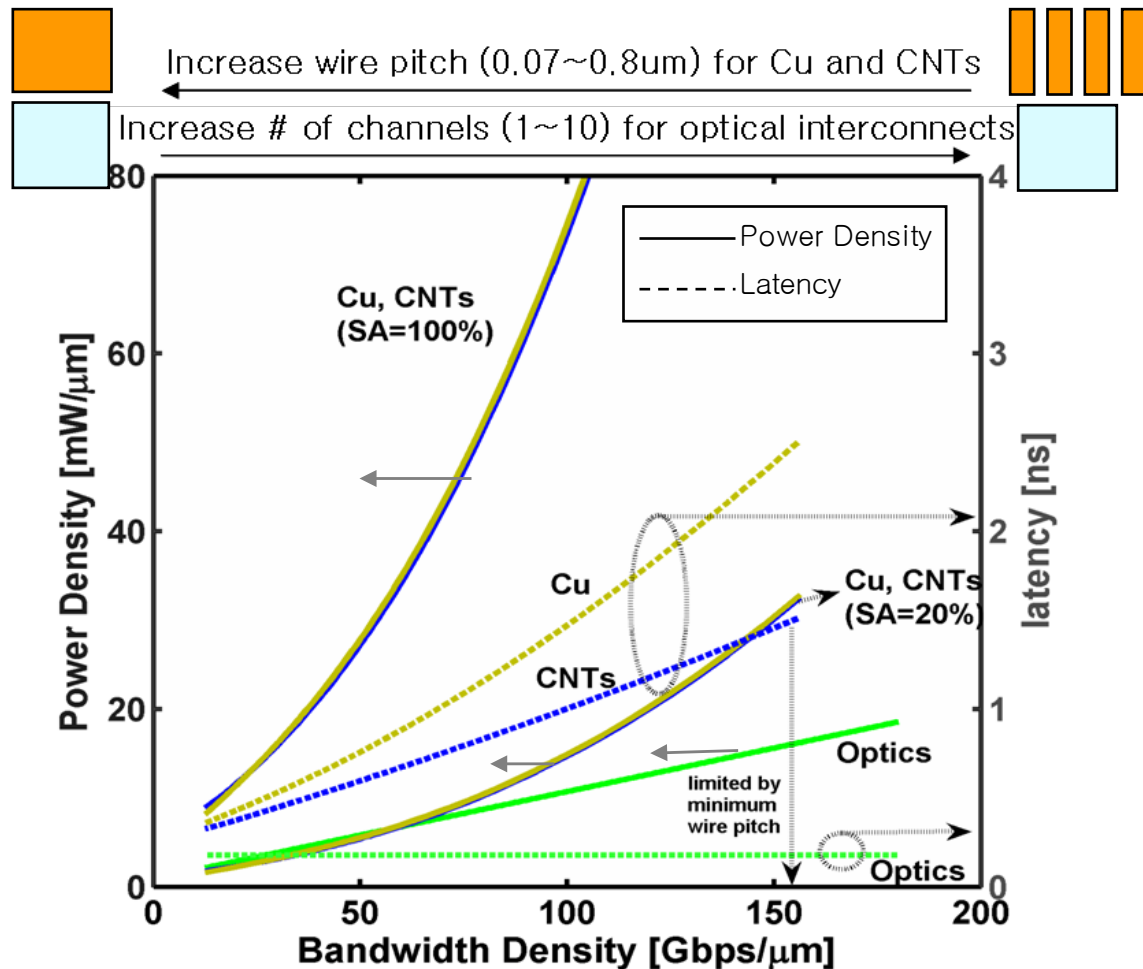
- Cu, CNT: small wire width  $\rightarrow$  more repeaters, wire capacitance  $\rightarrow$  latency  $\uparrow$
- CNTs are favorable for shorter wires
- Optics favorable for longer wires



- Cu, CNT: small wire width  $\rightarrow$  Energy per bit decreases as wire pitch is scaling ( $CV^2$ )
- CNTs is favorable for shorter global wire
- Optics: transmitter receiver power  $\downarrow$
- Optics favorable for longer wires



# Comparison Study: Global Interconnect CNTs, Cu, Optics



## - BW density

*Cu and CNTs:*  $f_{clk} / pitch_{wire}$

*Optics:* no. of wavelength of WDM

## - Power density

*Cu & CNTs (non-linear):*

*Cap and wire pitch*

*Optics (linear):*

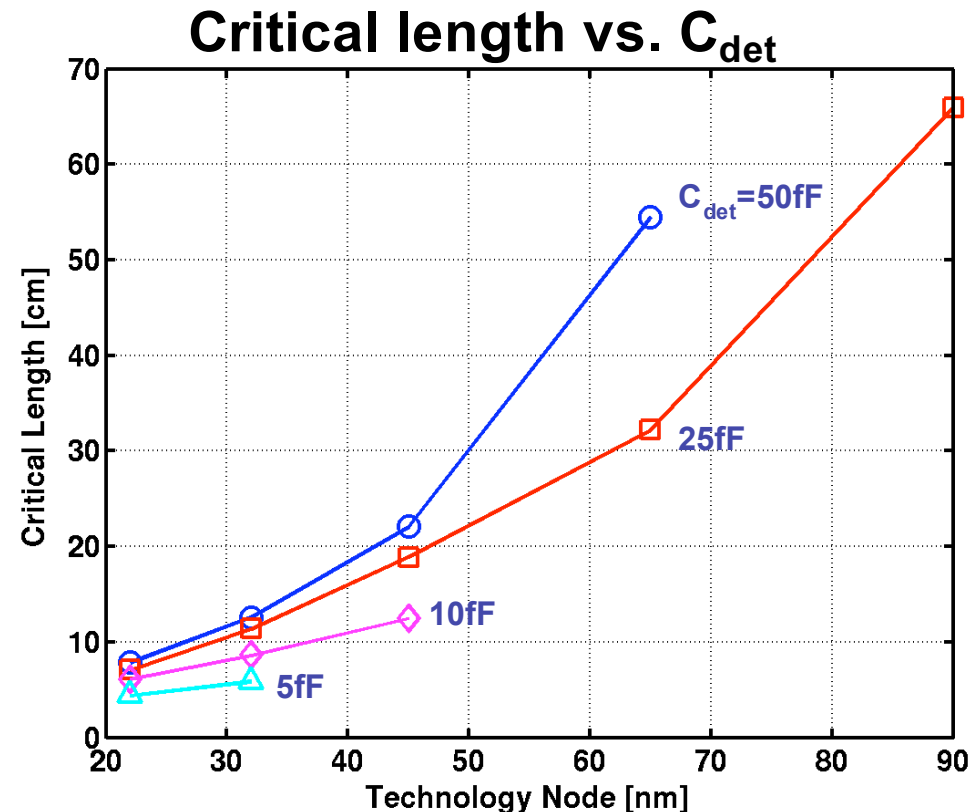
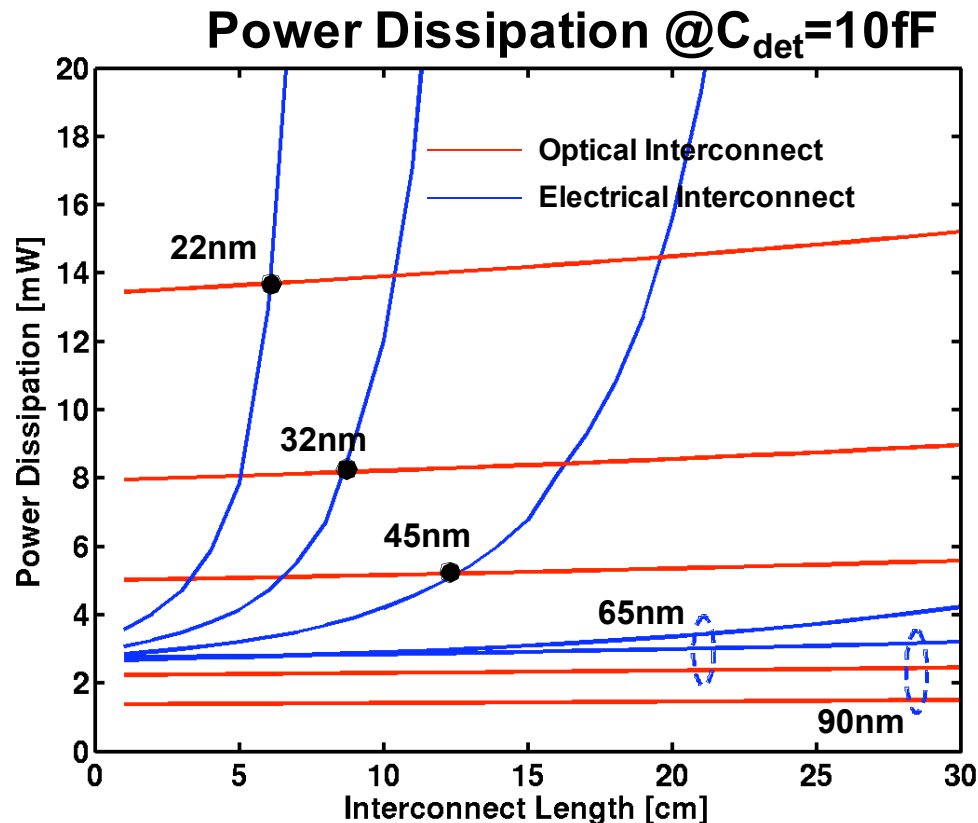
*no. of wavelength*

*channel*

## - Latency

Optics < CNTs < Cu

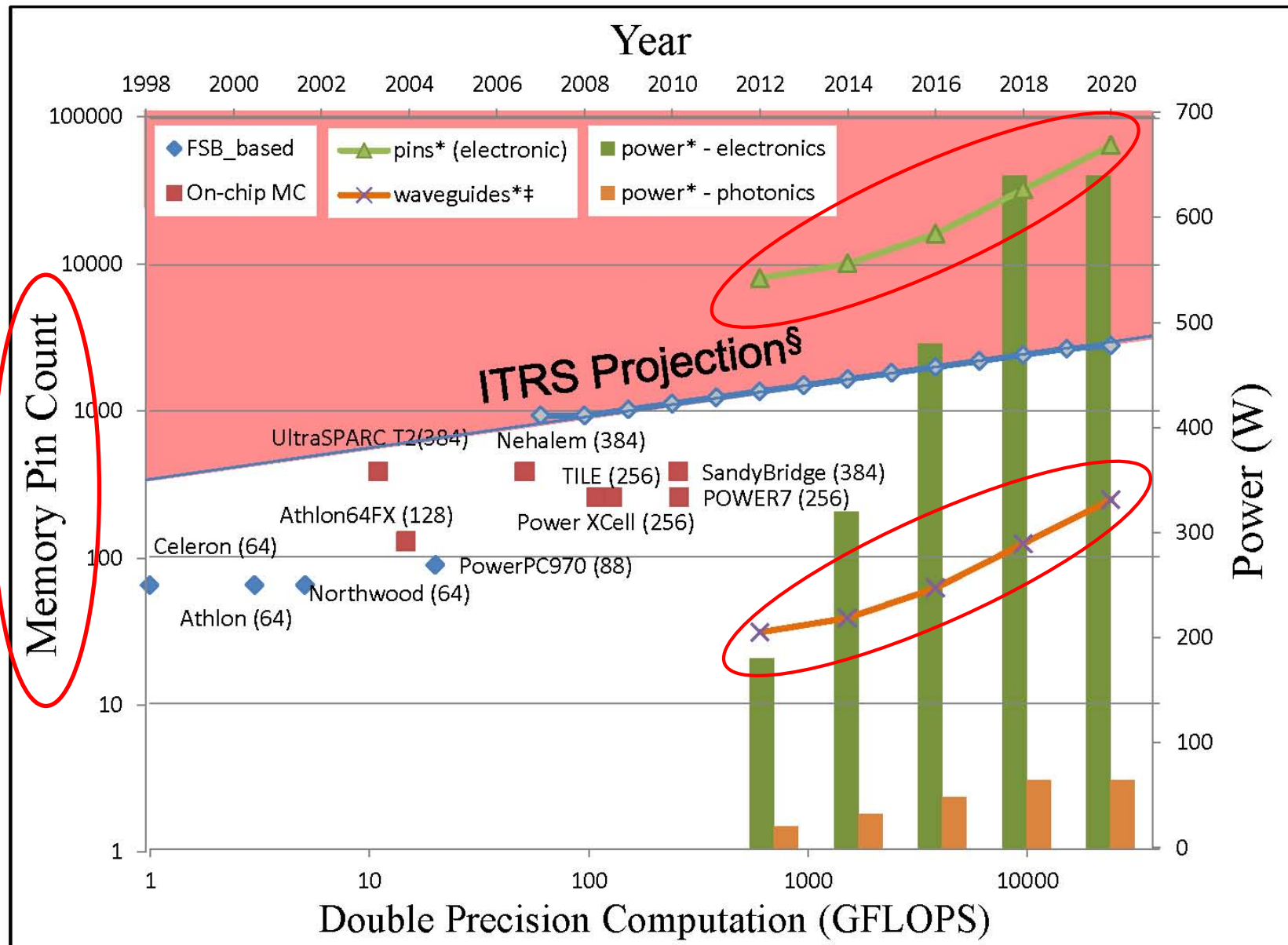
# Off-Chip Interconnect Performance: Electrical vs. Optical



- Beyond certain length optical I/O is more power efficient
- Critical length decreases at higher bit rate & **lower detector capacitance**
- **Beyond 32nm Technology node critical length < 10cm**

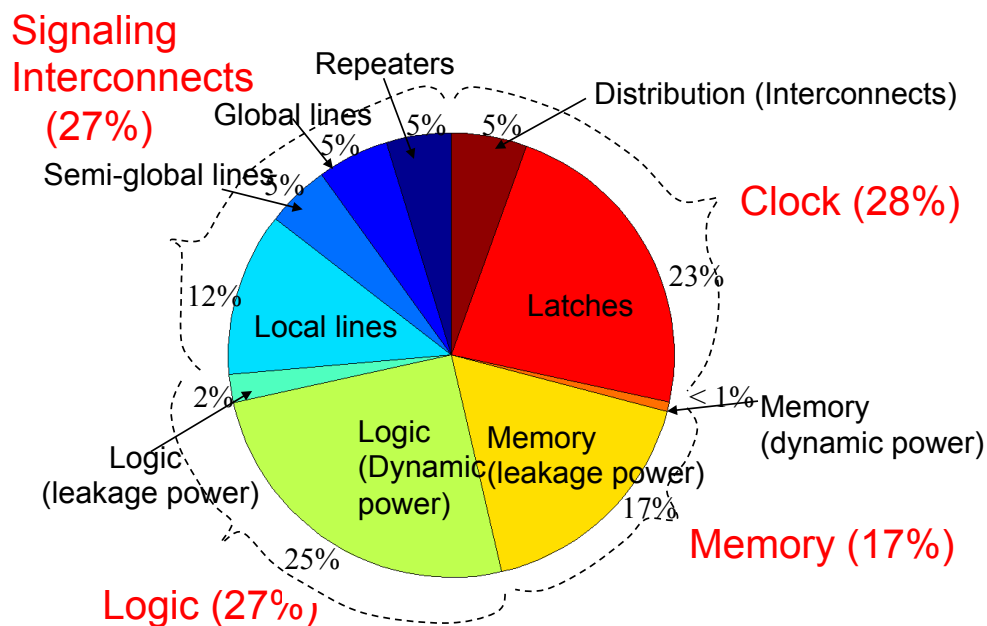


# Why Really Photonics?



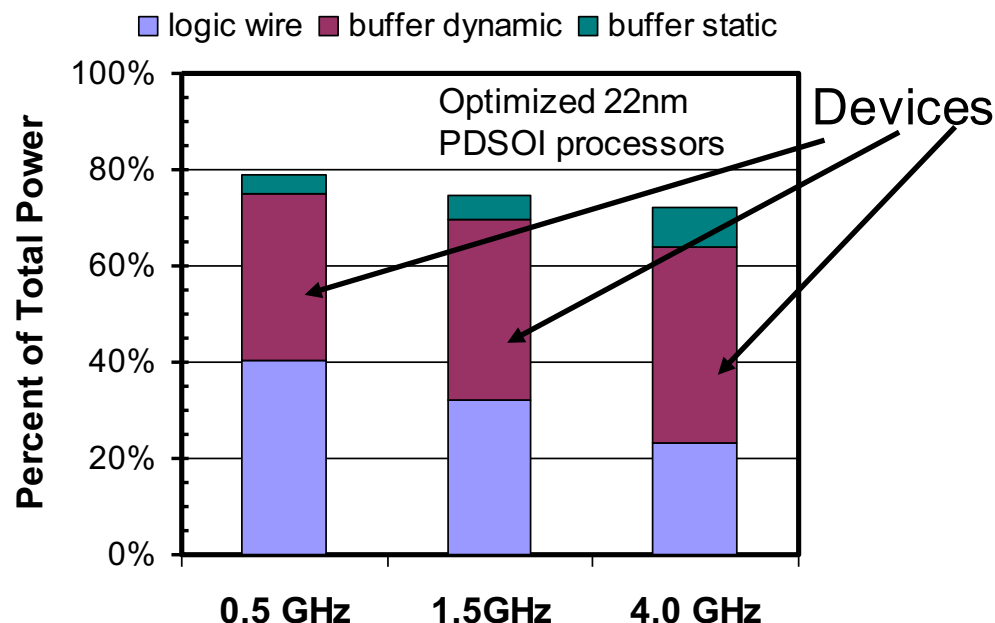
# Communication Dominates Power

## On-Chip Power Breakdown 50nm node



More than half the power can be attributed to interconnects

Chandra, Kapur and Saraswat,  
IEEE IITC, June 2002



70-80% of total logic power is for communication

– Need proper consideration of wires!!

Wilfried Haensch, (IBM) Data Abundant Systems  
Workshop, Stanford Univ., April 2014

# Why Off-chip Photonic Interconnects

## Copper wires



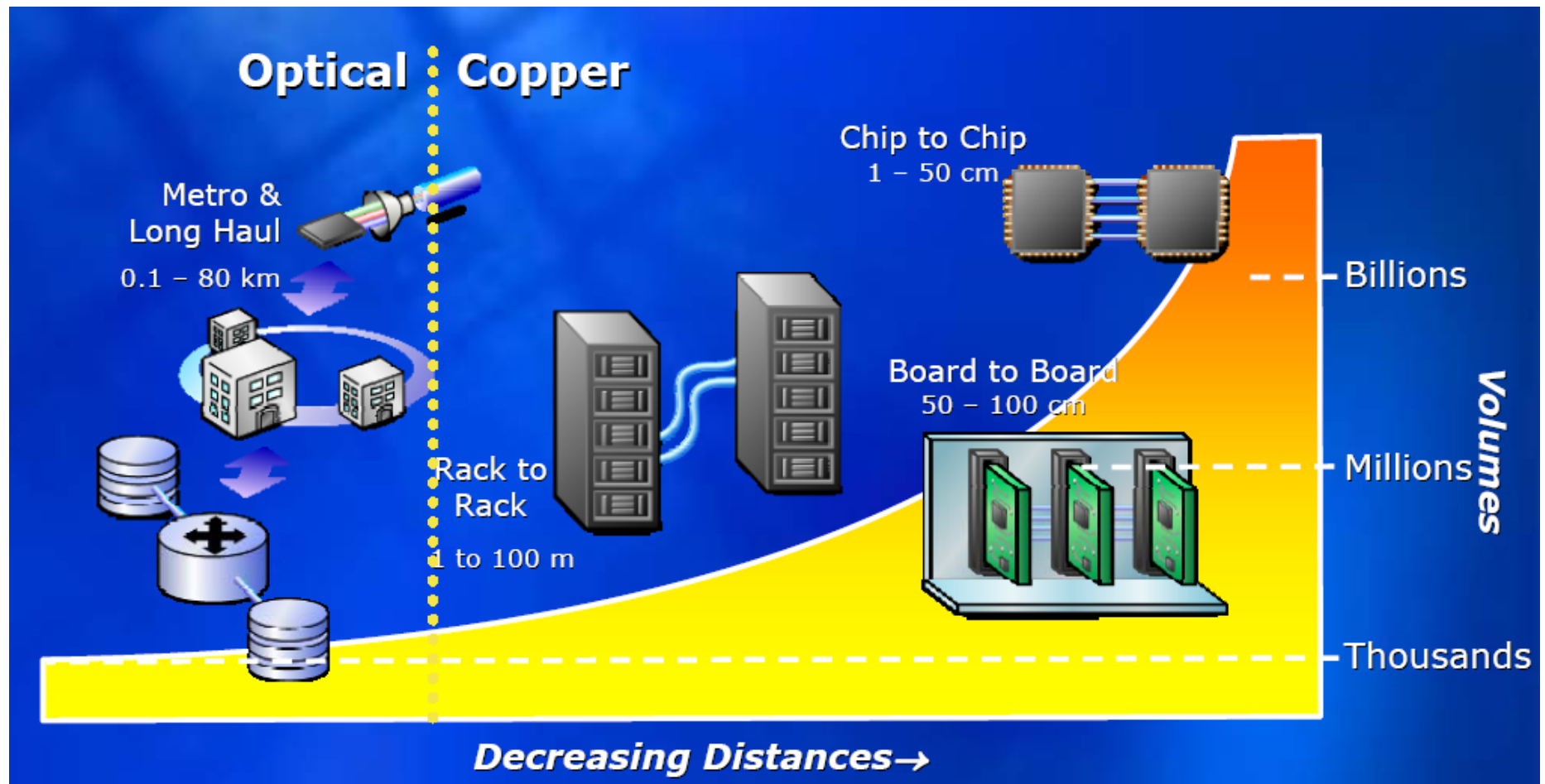
## Optical Interconnects



- Copper wires are reaching physical limits
- Photonic interconnects offer the solution for the future

# The Interconnect Problem

“For the long term, material innovation with traditional scaling will no longer satisfy performance requirements. Interconnect innovation with optical, RF, or vertical integration ... will deliver the solution” (ITRS)



# Material Options for Optical Interconnects

- What are the right optical devices to use?

- Need to be cheap, available in large numbers
- Compatible with CMOS

- Silicon devices are a long shot

- Need 3D heterogeneous integration

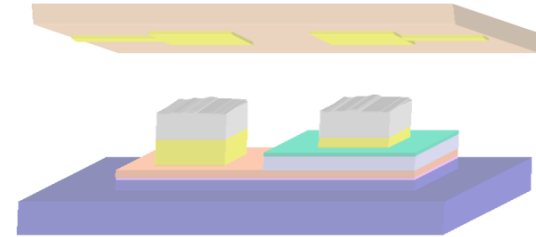
- Flip bond III-V to Si CMOS

- Current process
- Cost, resources, yield?

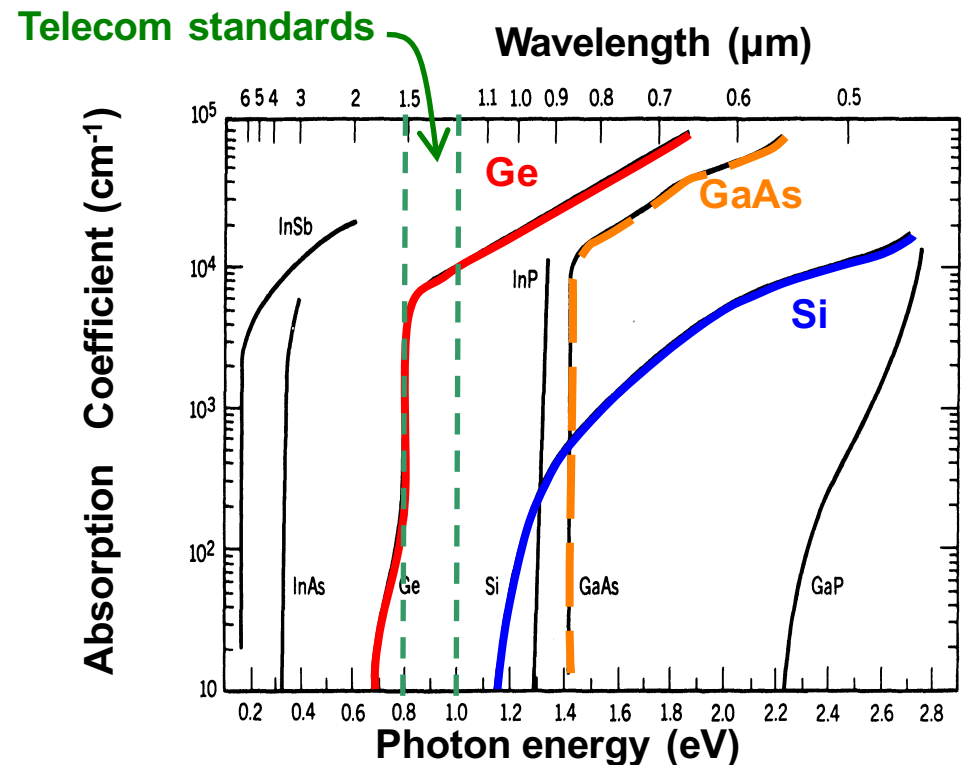
- How about germanium?

- Bandgap ideal for  $\lambda = 1.5 \mu\text{m}$
- Can be monolithically integrated on Si
- Becomes direct bandgap material by straining or adding tin

Si CMOS chip with gold bonding pads

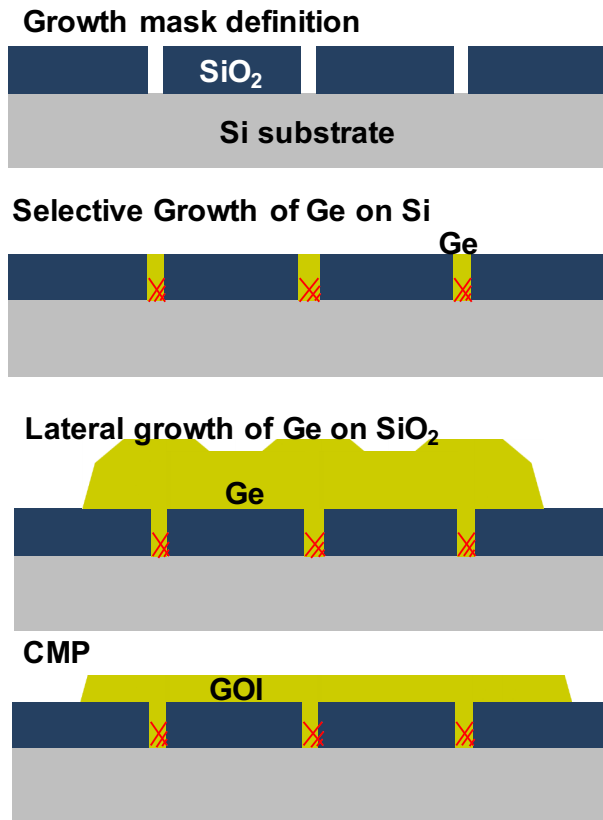


GaAs optoelectronic chip with indium flip-chip bumps

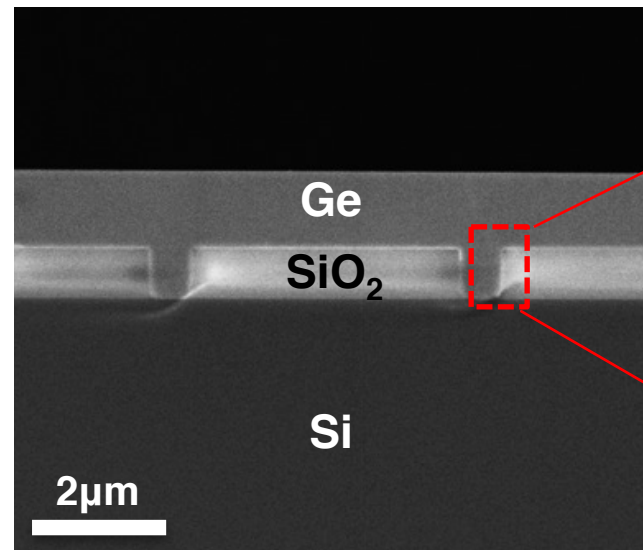




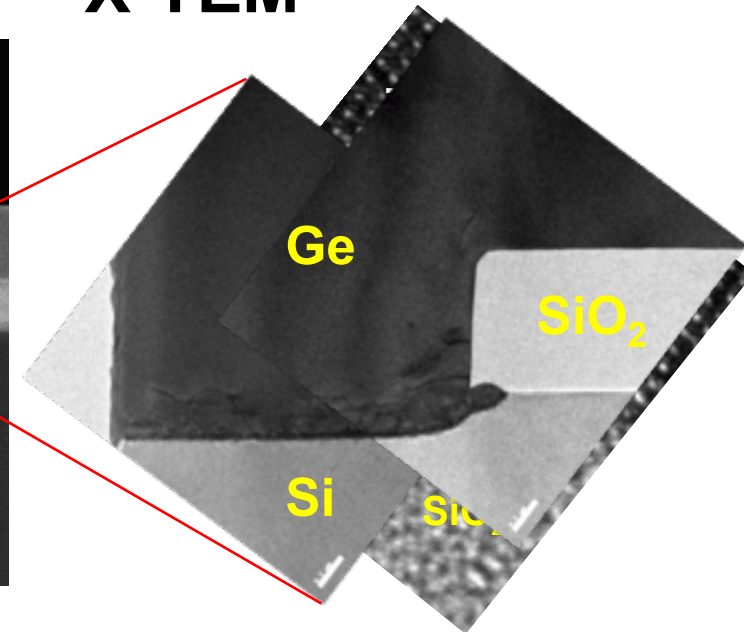
# Selective and Lateral Overgrowth of Ge on SiO<sub>2</sub>



**SEM**



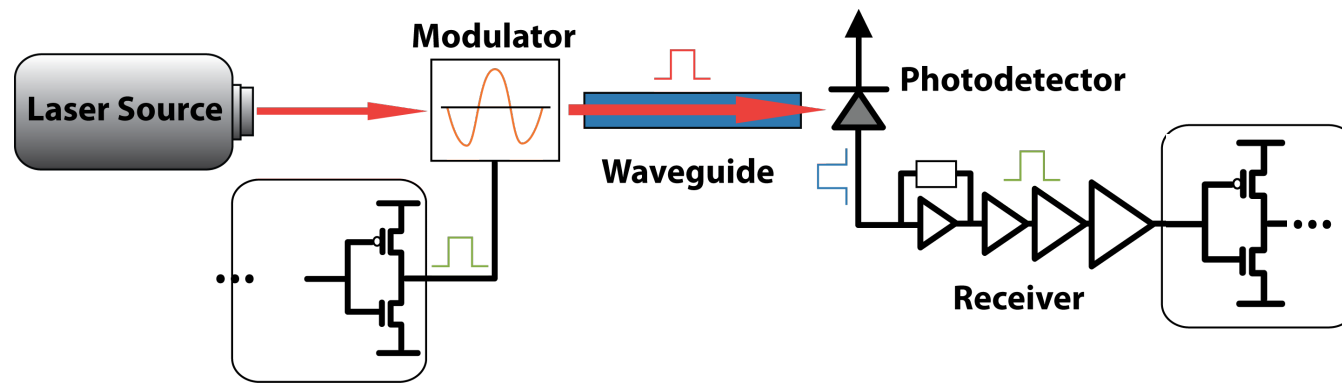
**X-TEM**



400°C deposition + 800°C H<sub>2</sub> anneal + 600°C deposition

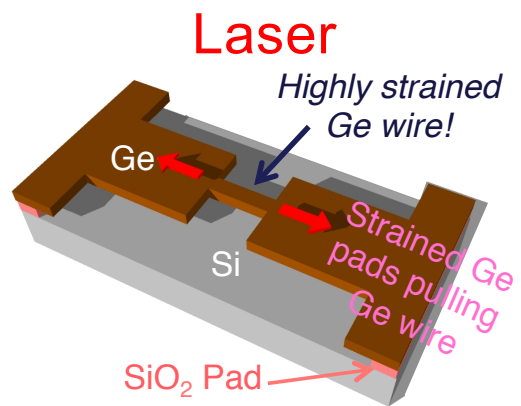
- Lateral Ge growth on SiO<sub>2</sub> window achieved
- Dislocation density of Ge on SiO<sub>2</sub> < 10<sup>6</sup> cm<sup>-2</sup> (same thickness Ge on Si: 1 × 10<sup>8</sup> /cm<sup>2</sup>)
- Surface RMS roughness ~0.4 nm after CMP
- Ge is ~0.2% tensile strained due to thermal mismatch with Si

# Si Compatible Photonic Interconnect

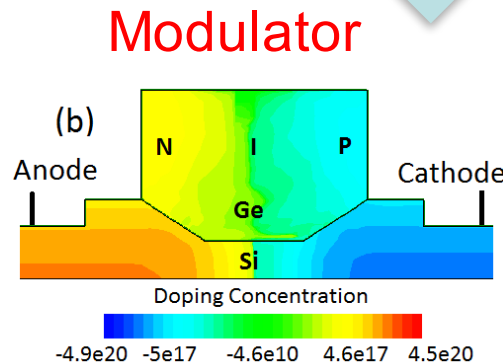


Laser/modulator converts electrical signal into optical signal

Photodetector restores optical signal into electrical signal

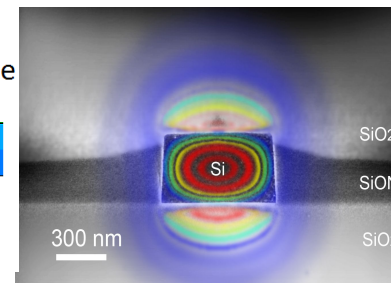


Nam.....Saraswat,  
Nano Letters, June 11, 2013.

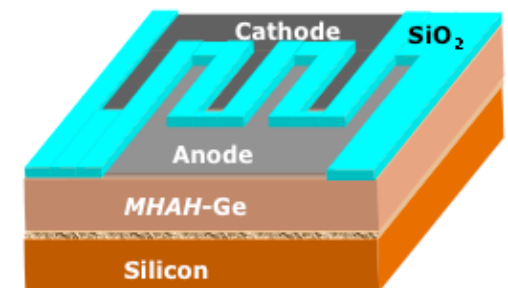


Gupta.....Saraswat,  
OFC, March 2015

Waveguide



Detector

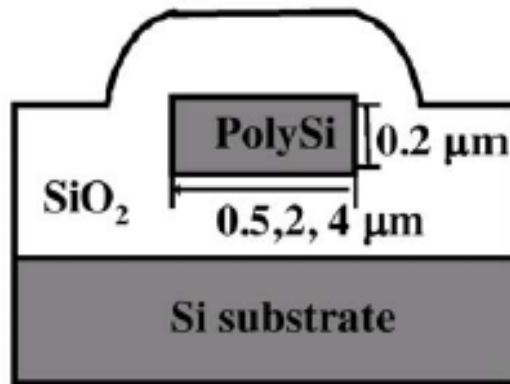


Okyay..... Saraswat,  
Optics Lett. 2006

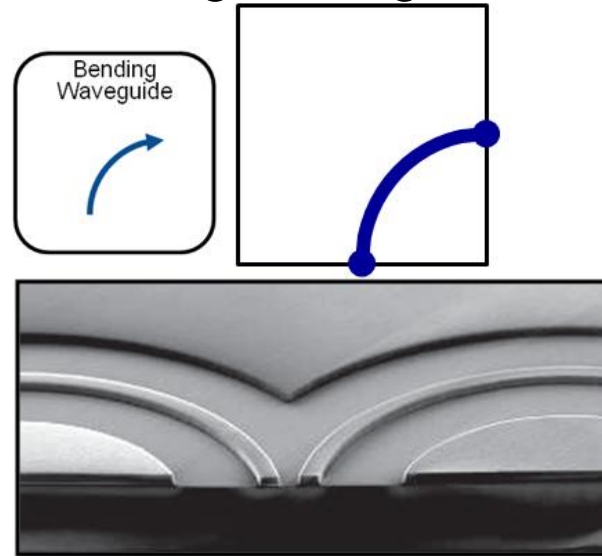
- Germanium devices can be monolithically integrated on silicon
- Laser is the only missing component

# Technology for Optical Interconnects on Silicon: Optical Transmission Media

Waveguides

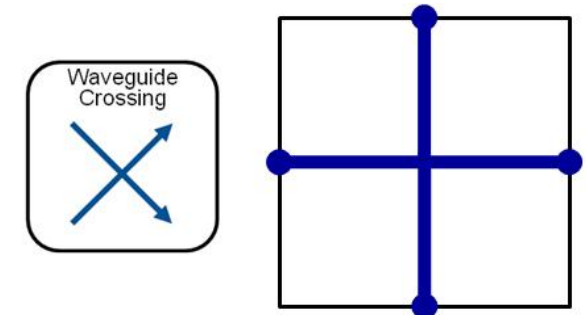


Bending Waveguides

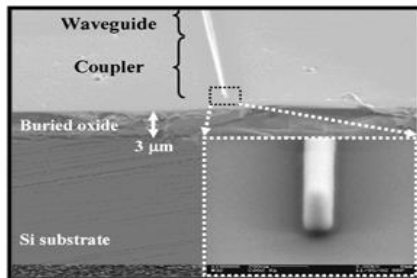
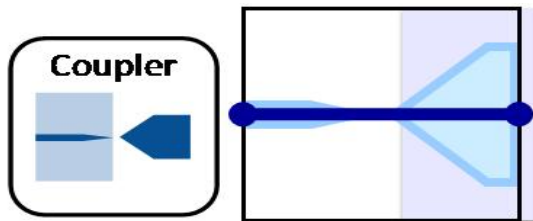


[F. Xia et al., Nature Photonics, 2006]

Waveguide Crossings

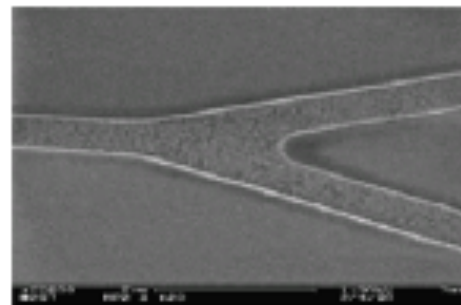


Couplers

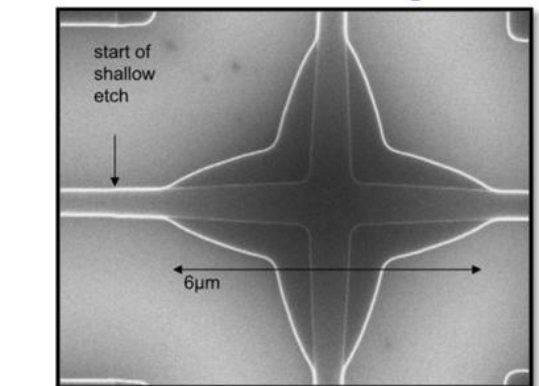


[V. Almeida et al., Optics Letters, 2003]

Splitter



(Kimmerling, MIT)

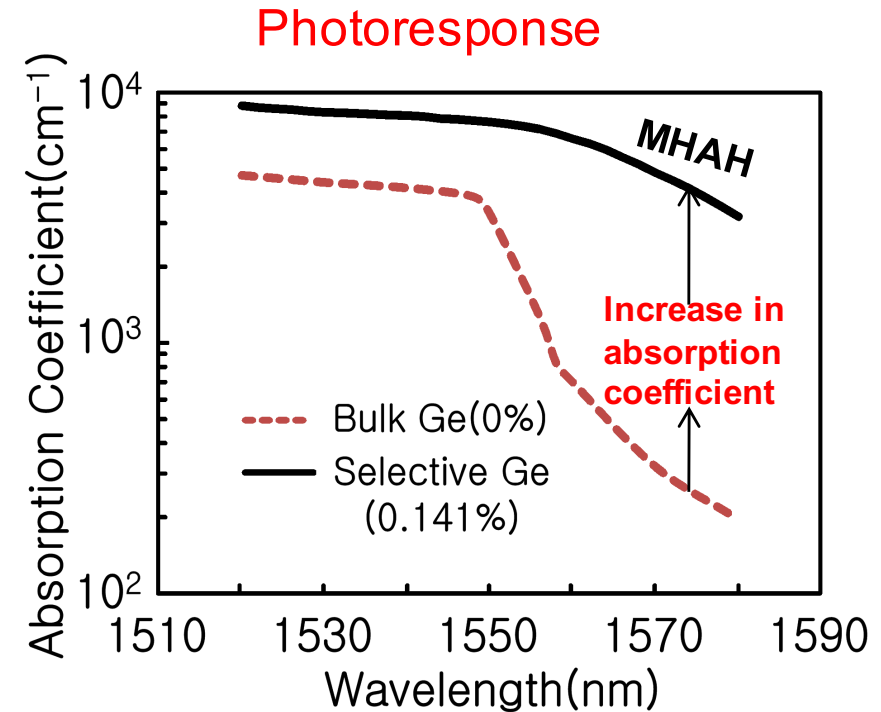
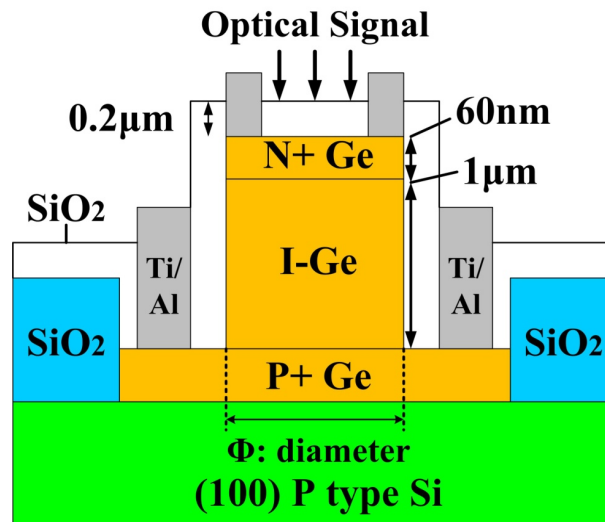
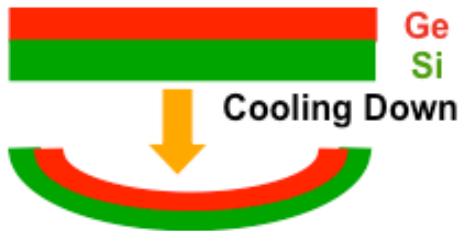


[W. Bogaerts et al., Optics Letters, 2007]



# High Efficiency Ge p-i-n Photodetectors on Si

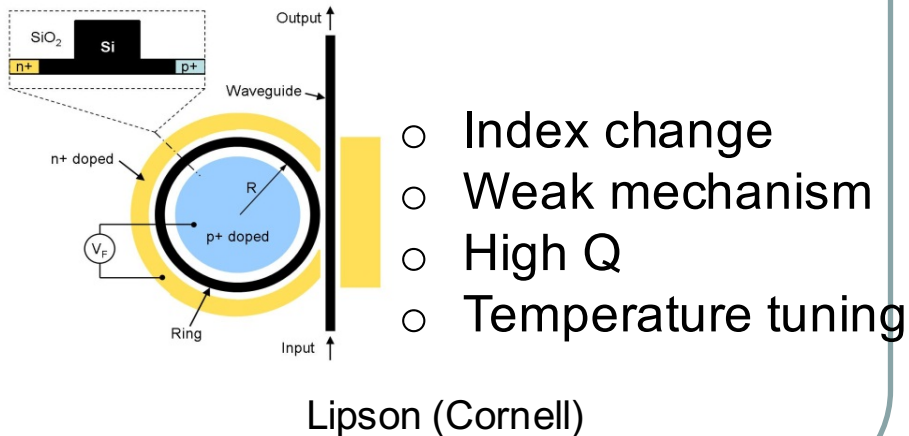
Biaxial Tensile Strain



- Ge grown on Si by **M**ultiple **H**ydrogen **A**nneal and **H**eteroepitaxy (MHAH) Technique
- Ge film complies with Si substrate on cooling down resulting in tensile strain => bandgap reduces
- Detector efficiency improves at 1550nm due to tensile stress
- **Dark Current high**

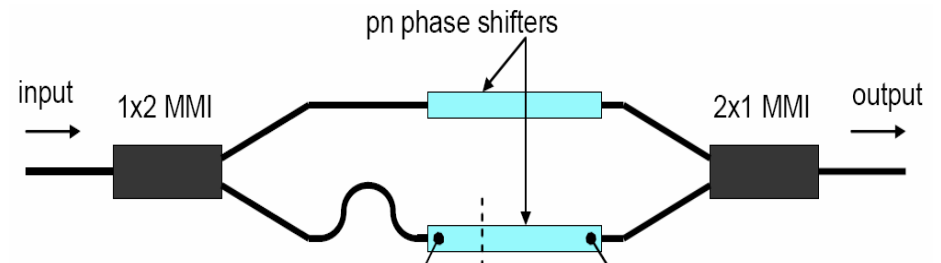
# Optical Modulator

## Electro-optic Modulators



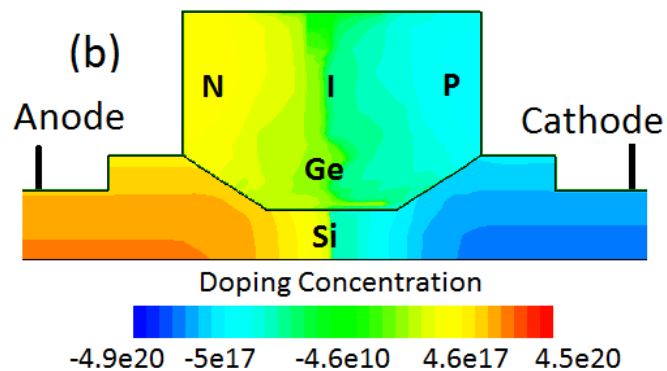
## Mach-Zehnder Modulators

- Phase shift effect in waveguides
- Large size and power consumption



## Electro-absorption Modulators

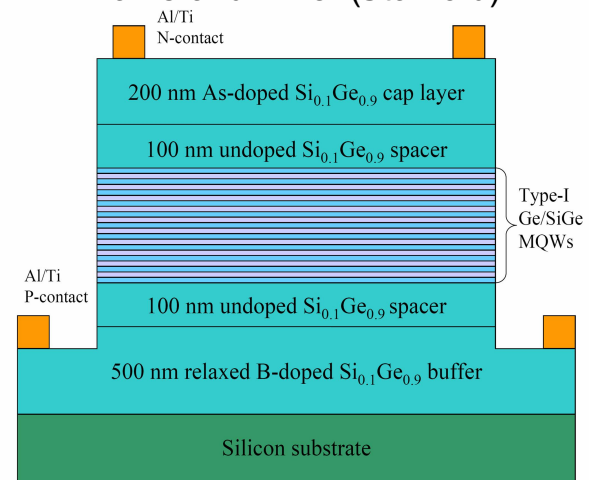
Saraswat (Stanford)



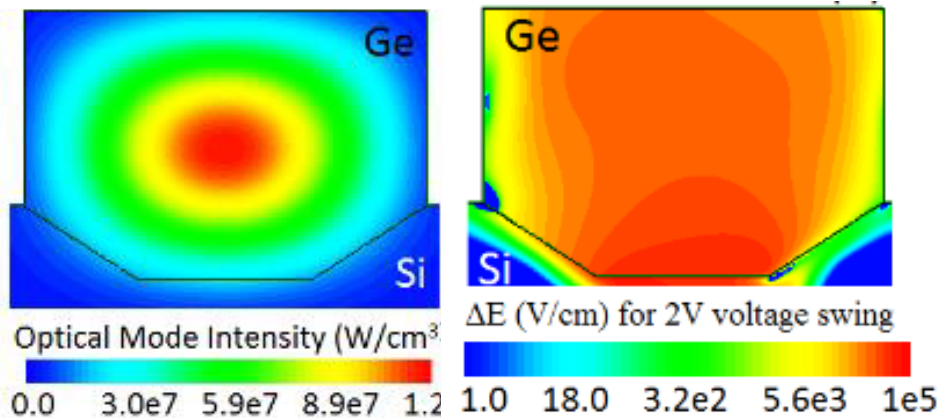
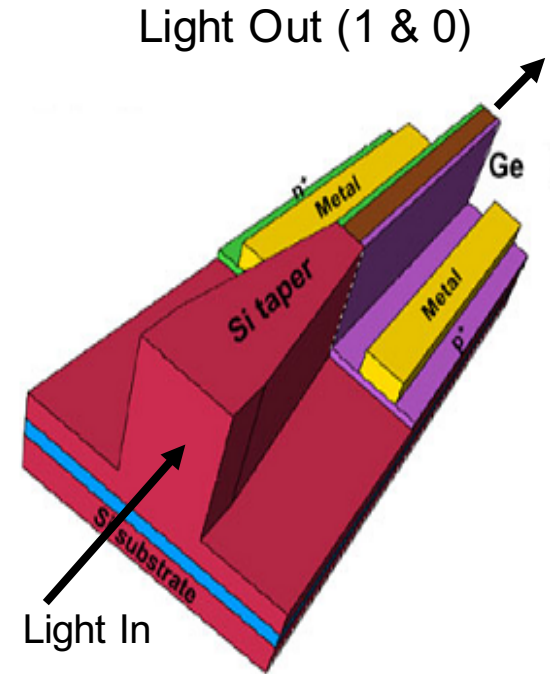
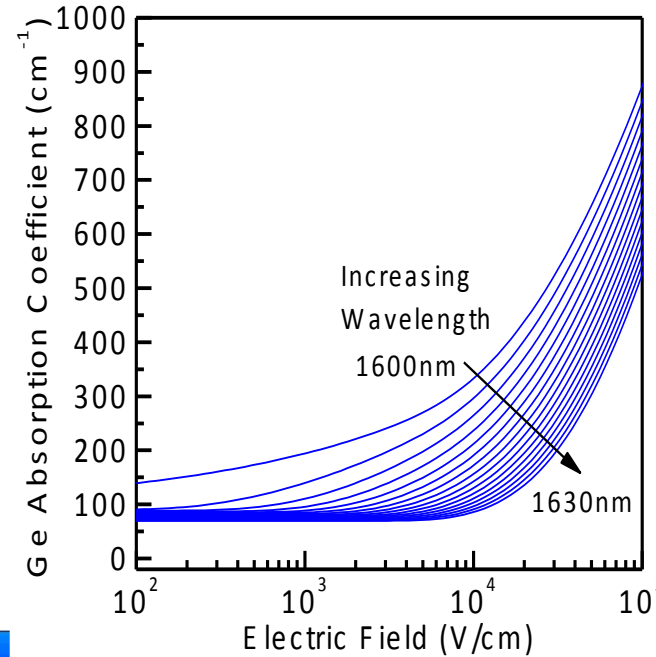
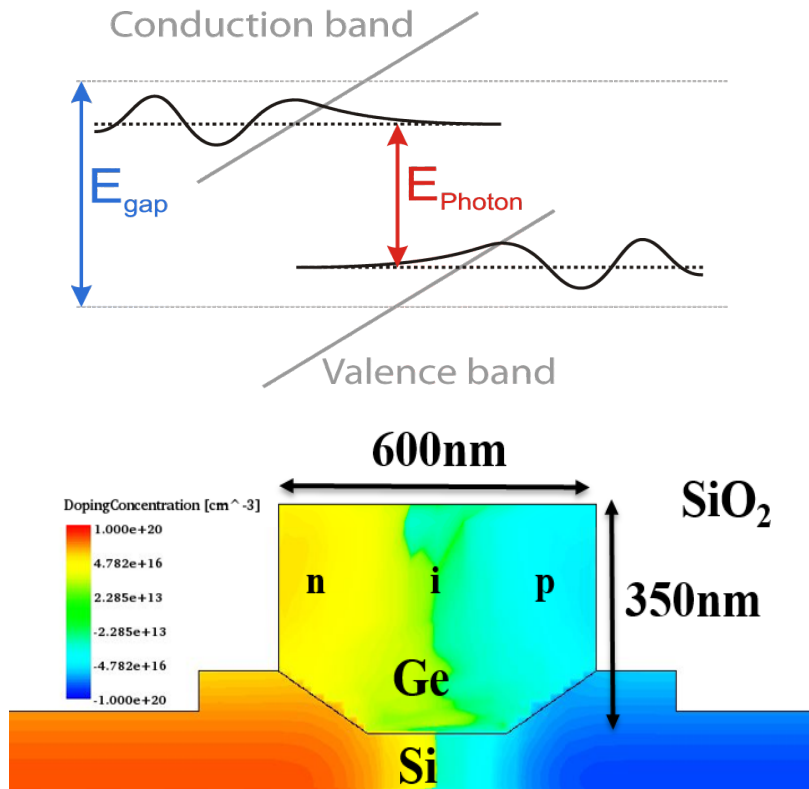
- Franz-Keldysh effect in bulk material

## QCSE Ge/SiGe Modulator

Harris and Miller (Stanford)



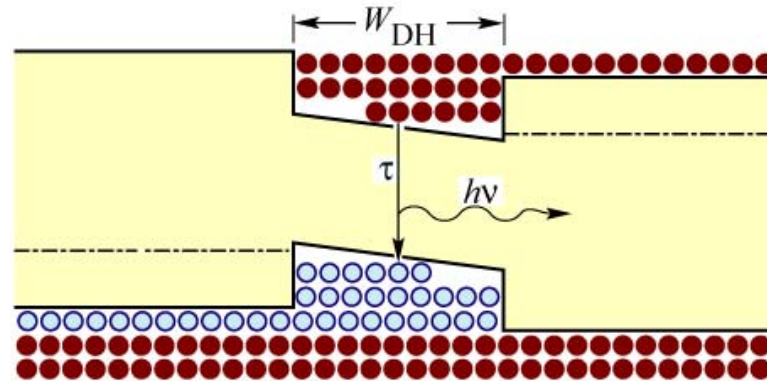
# Ge/Si Electro-Absorption Franz-Keldysh Effect Modulator



In the presence of an electric field, the conduction and valence bands of a semiconductor tilt. Application of an electric field leads to overlap in valence and conduction band wave functions, and hence optical absorption, at energies below the semiconductor bandgap.

# Structure Needs for Efficient Lasing

## Heterojunction



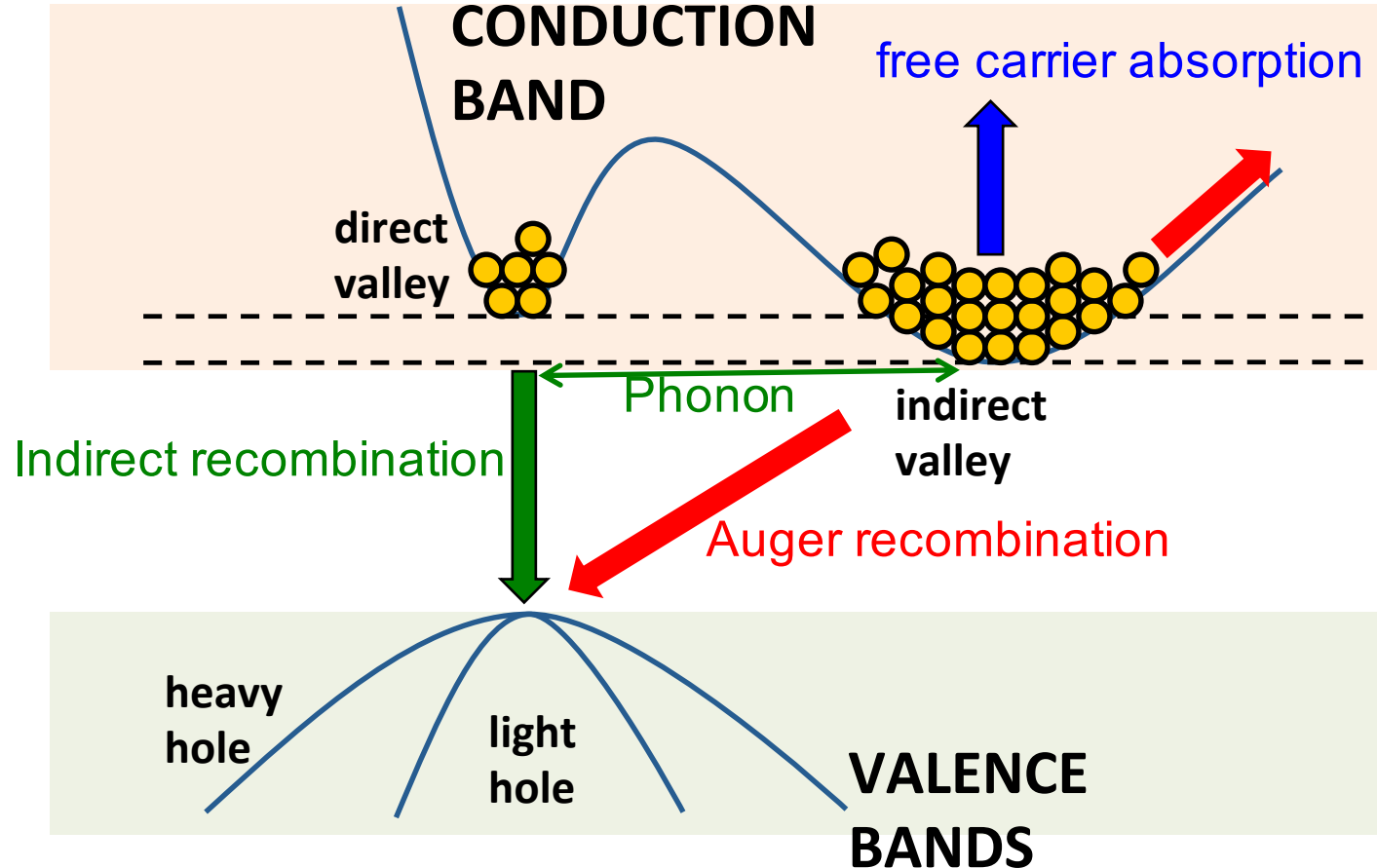
For efficient laser

- Direct bandgap cavity
- Heterojunction quantum well for carrier confinement

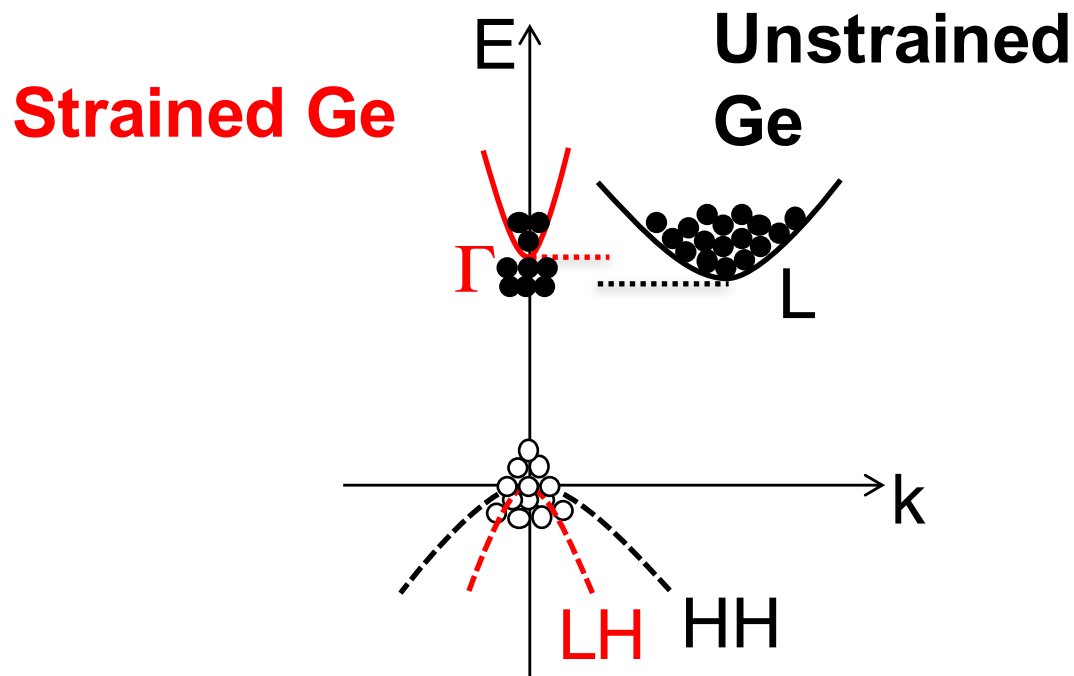
E. F. Schubert, Light Emitting Diodes (Cambridge Univ. Press)

# Engineering Ge for light emission- Doping

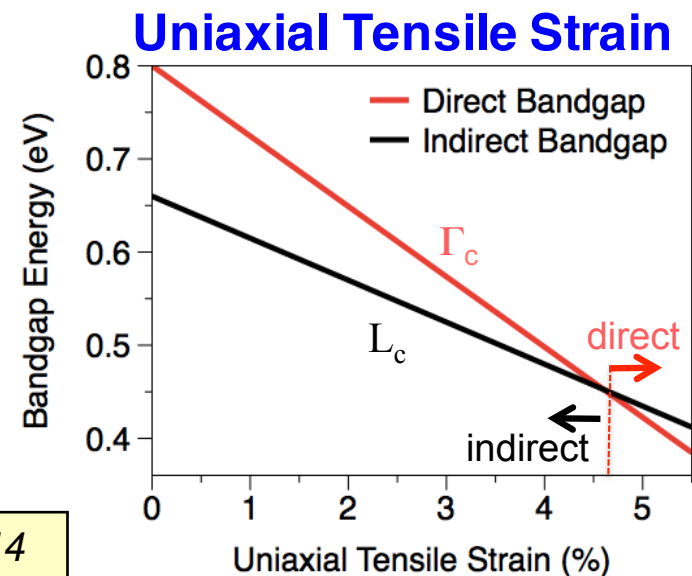
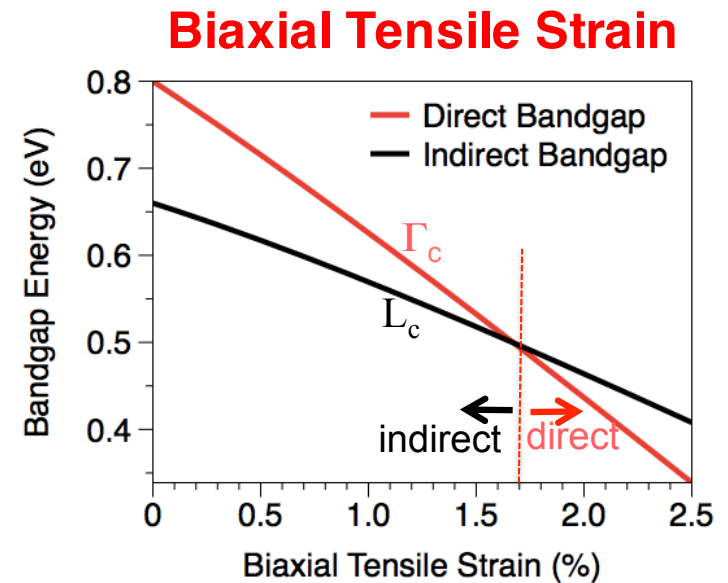
- N-type doping can be used to fill electrons into the L valley upto the level of  $\Gamma$  valley
- But it is difficult to heavily dope Ge n-type
- Increases free carrier absorption and auger recombination
- **Inefficient light emission**



# Engineering the Ge band structure for light emission: Strain

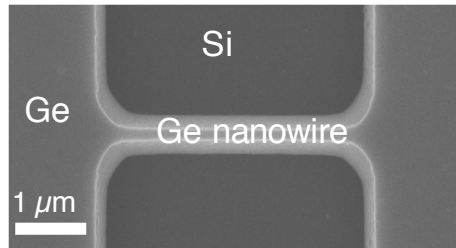


>1.7% biaxial tensile strain or  
> 5% uniaxial tensile strain  
turns Ge into a direct bandgap  
material, making light  
emission possible

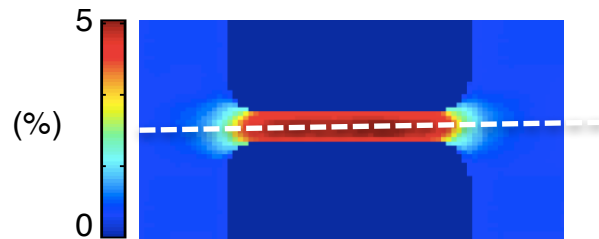


# Heterostructure in a Single Material: Strained Ge

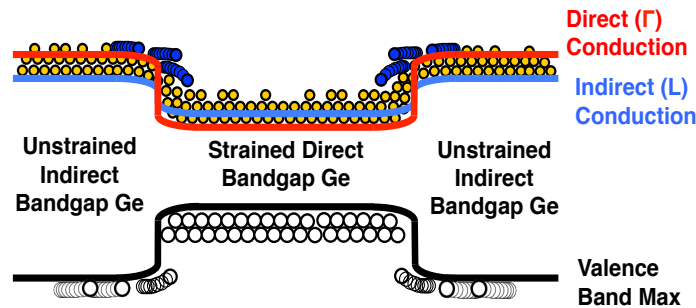
SEM



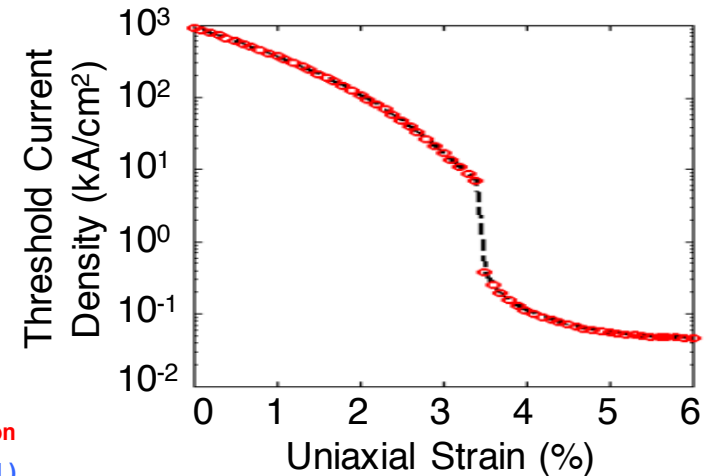
2D Strain Distribution



Band Diagram



Threshold Current Simulations



- Strain can be tunable with geometry
- Heterostructure created due to reduction in bandgap of strained Ge
- Direct bandgap cavity and heterojunction quantum well in single material



# Engineering the Ge band structure by alloying with tin for GeSn CMOS and photonics

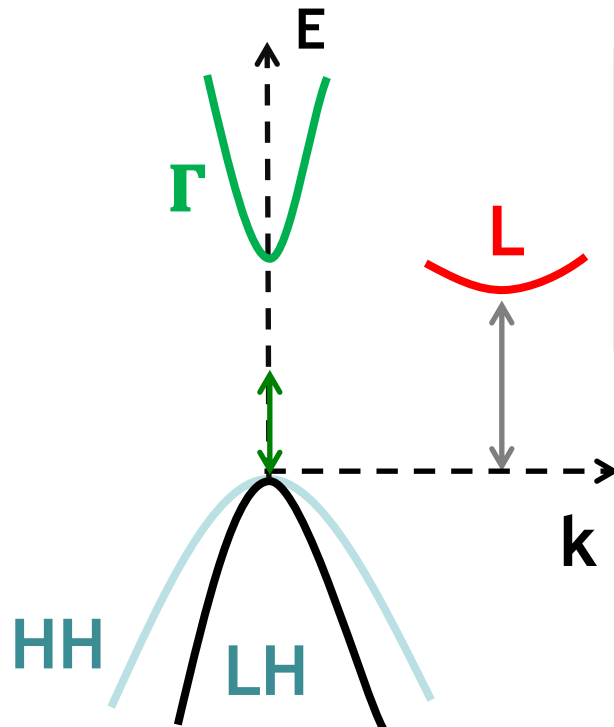
14	2	8	4
<b>Si</b>	5.43 Å		
Silicon	28.0855		

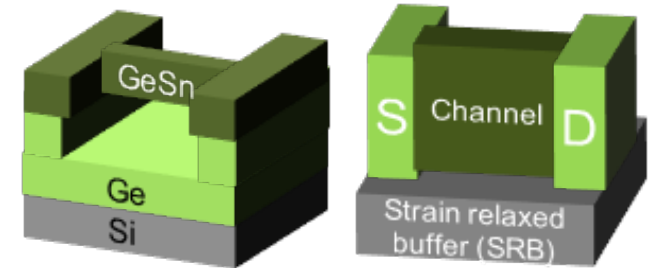
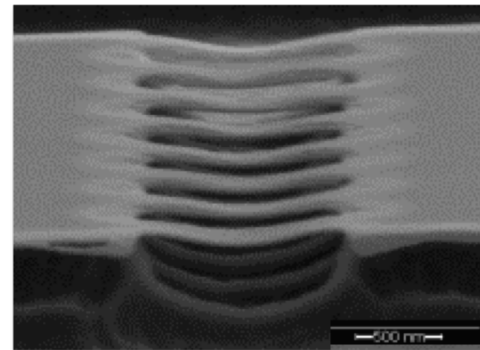
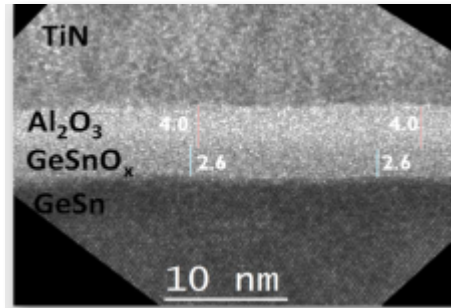
32	2	8	18	4
<b>Ge</b>	5.65 Å			
Germanium	72.63			

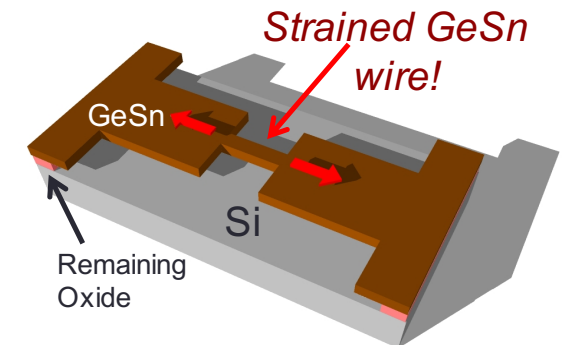
50	2	8	18	18	4
<b>Sn</b>	6.49 Å				
Tin	118.710				



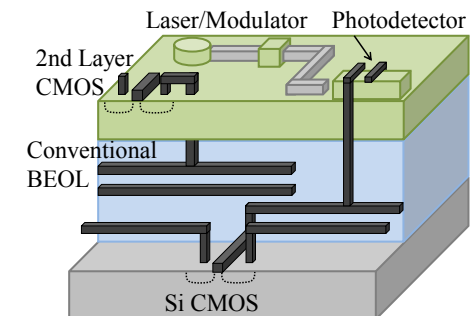
At ~ 7 Sn%  $\text{Ge}_{1-x}\text{Sn}_x$  becomes direct band gap!



Strain engineering in FinFETs



Si-compatible Laser

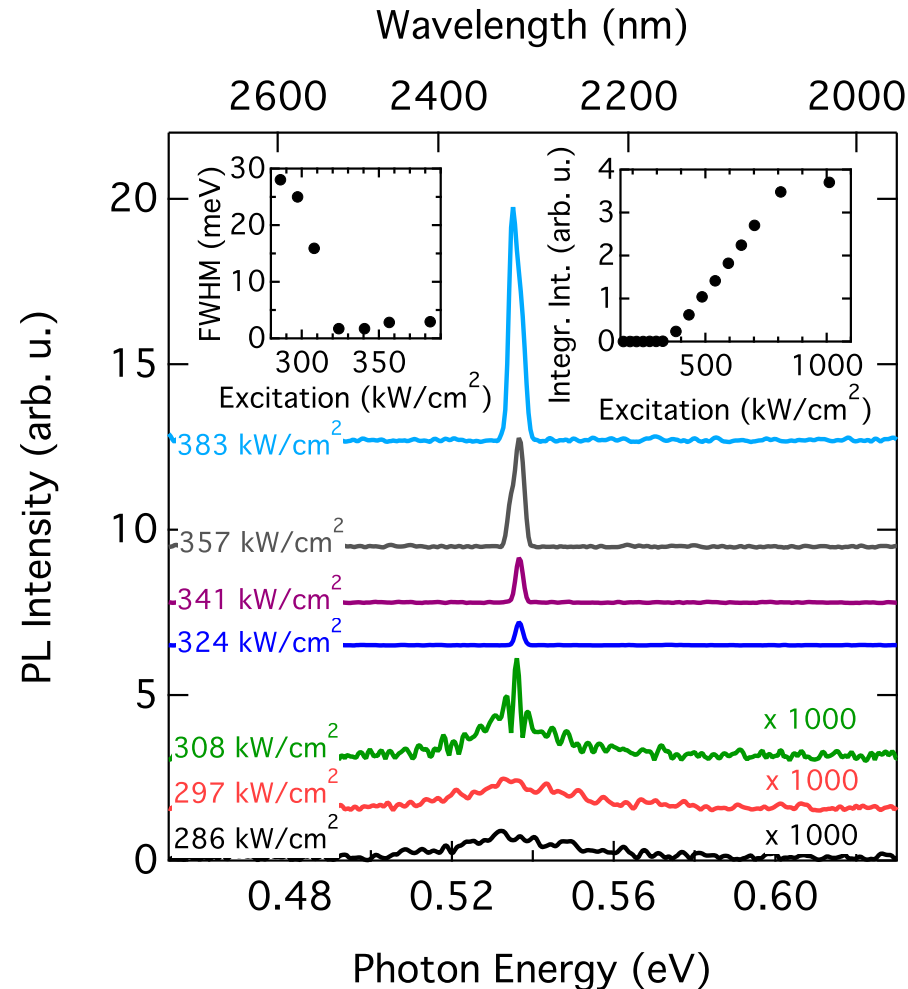


Gupta, Yeo, Takagi, Saraswat, et al.,  
MRS Bulletin, Aug 2014

3-D IC: CMOS, Photonics co-integration

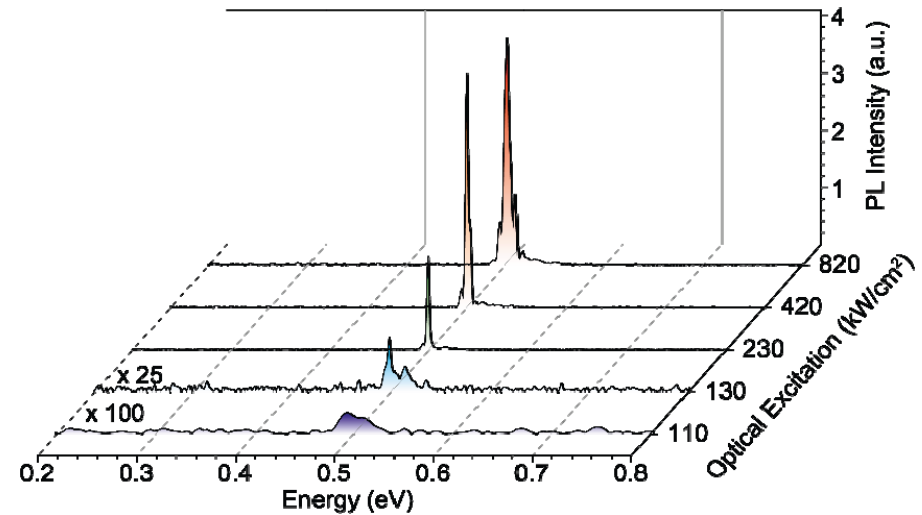
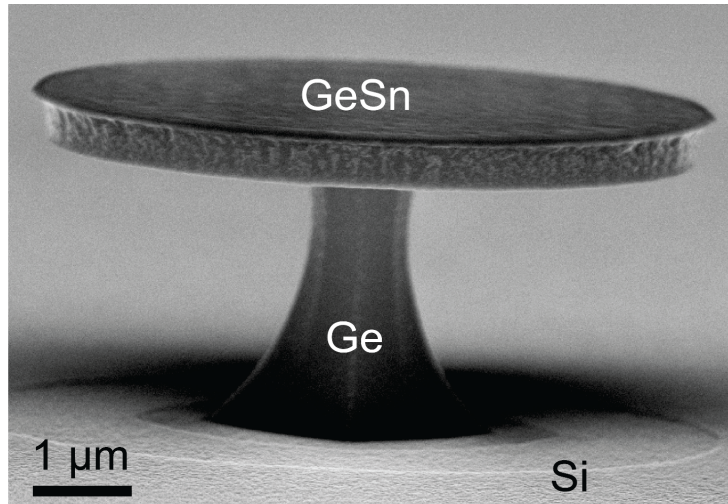


# Demonstration of Optically Pumped GeSn Laser



- Lasing emission spectra measured from the facet of a 5  $\mu\text{m}$  x 1 mm long Fabry-Perot waveguide  $\text{Ge}_{0.87}\text{Sn}_{0.13}$  cavity under optical pumping at 20 K.
- More work needed for room temperature laser

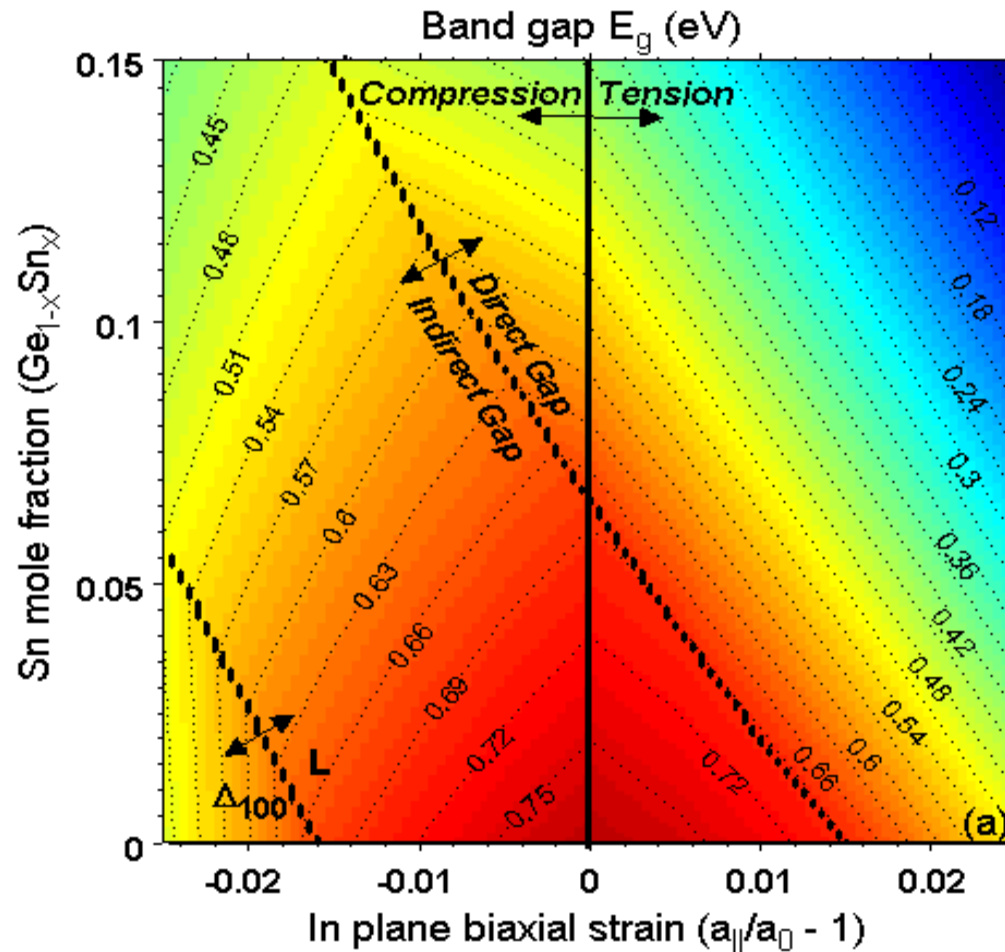
# Direct Bandgap GeSn Microdisk Laser on a Si-Platform



- Power-dependent PL spectra of an 8 μm diameter Ge<sub>0.875</sub> Sn<sub>0.125</sub> microdisk at 50 K.
- More work needed for room temperature laser

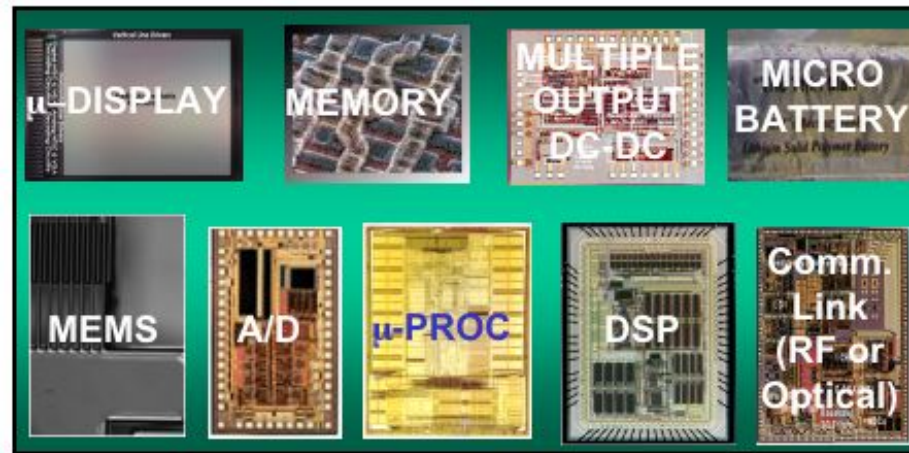
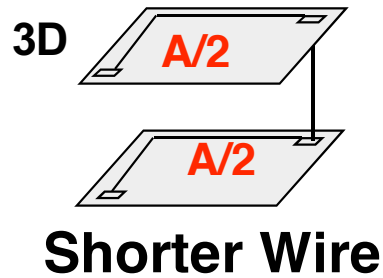
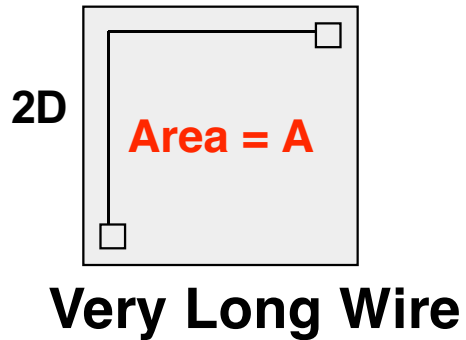
S. Wirth, et al., IEEE IEDM, Dec. 2015

# Multiple Knobs to Turn for Direct-Gap: Strained GeSn

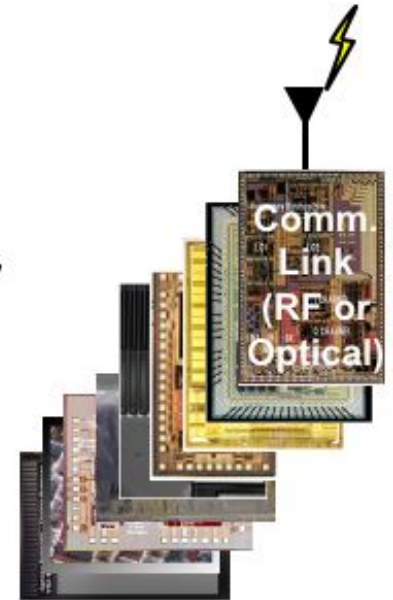


- A combination of alloying Ge with Sn and strain can also give us a direct bandgap material
  - Efficiency would be comparable to present III-V lasers

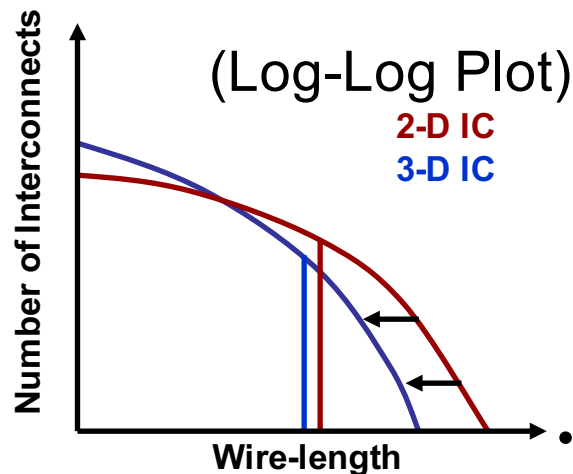
# 3-D Integration: Motivation



2-D System



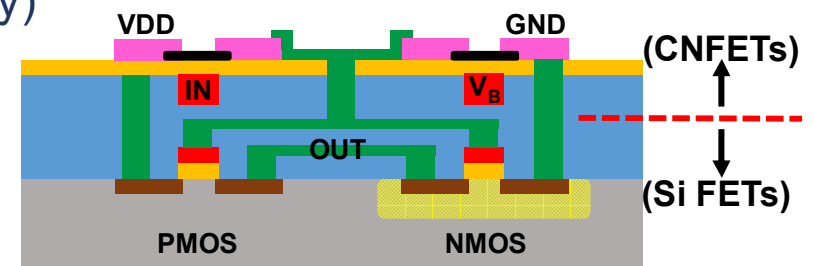
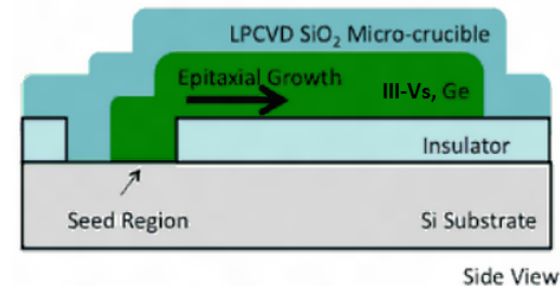
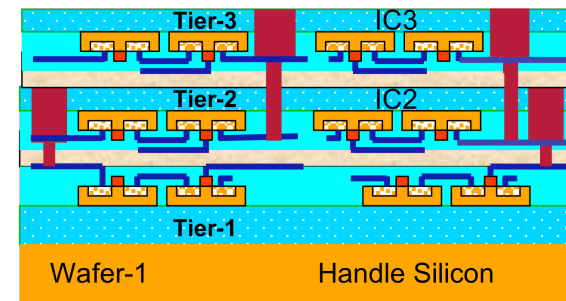
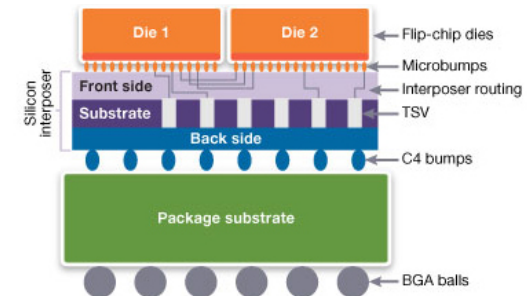
3-D System



- Reduce Chip footprint
  - Improved form factor
  - Interconnect length ↓ and therefore R, L, C ↓
    - Delay reduction
    - Power reduction
    - Higher bandwidth
- Integration of heterogeneous technologies possible, e.g., memory & logic, sensors, optical I/O

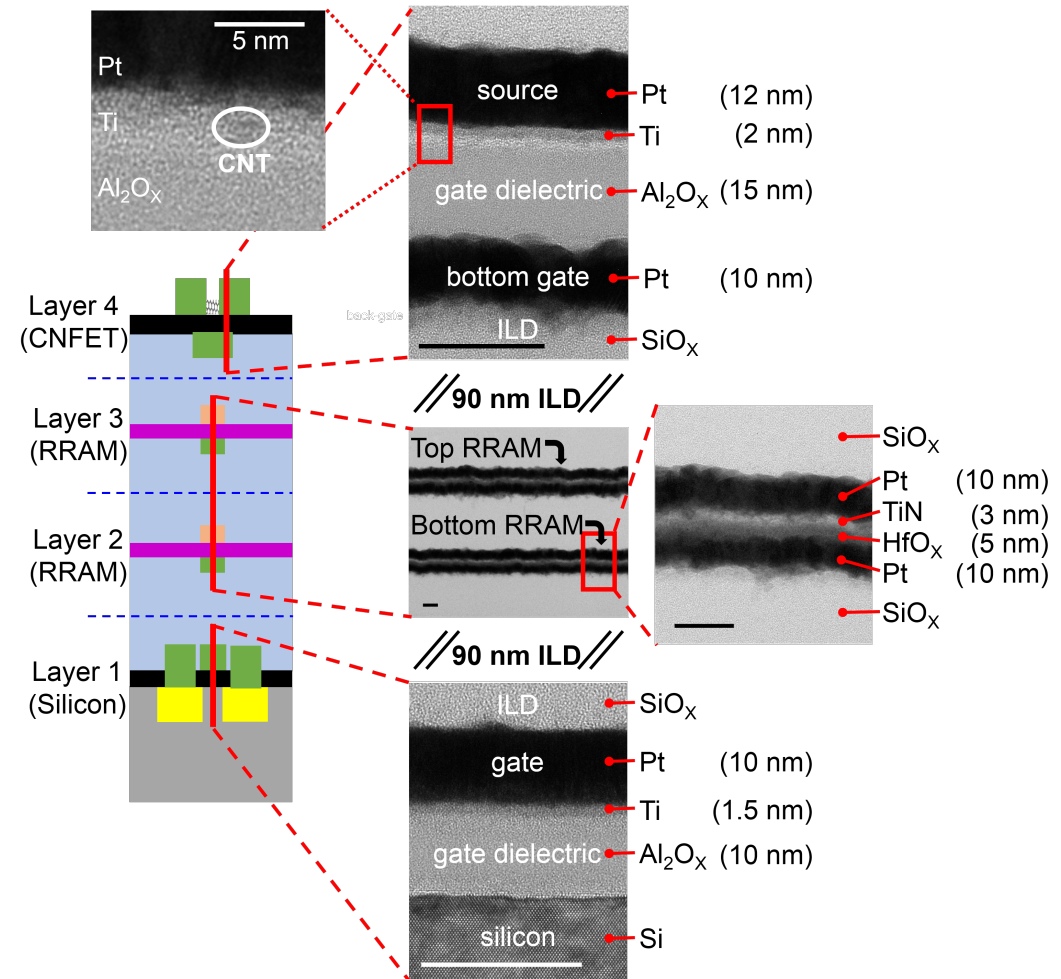
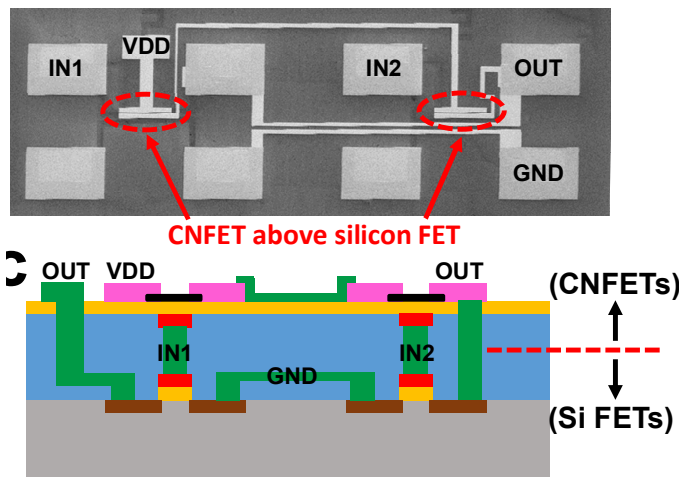
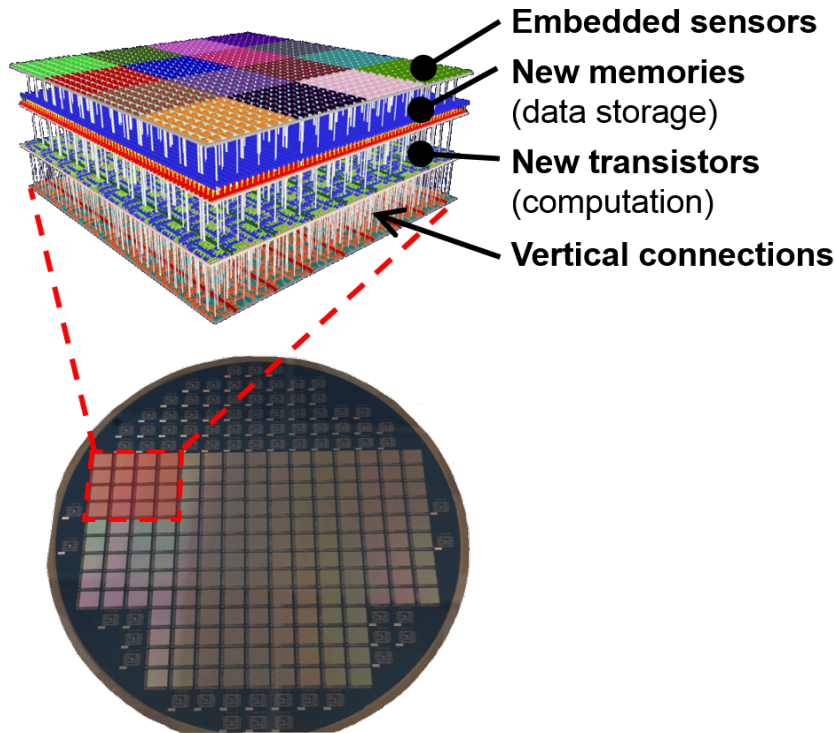
# Technology to Fabricate 2.5D/3D ICs

- **2.5D packaging** (mature technology)
  - Wire bonded
  - Bump
  - vertical interconnect density < 20/mm or 400/mm<sup>2</sup>
- **3D bonding/TSV** (emerging technology)
  - Die stacking
  - wafer stacking
  - vertical interconnect density < 40,000/mm<sup>2</sup>
- **3D crystallization** (near future technology)
  - Epitaxial growth
  - Laser melting and crystallization
  - Seeded crystallization
  - Liquid phase crystallization
  - vertical interconnect density < 25M/mm<sup>2</sup>
- **3D self assembled devices** (future technology)
  - Si and Ge nanowires
  - Carbon nanotubes
  - Organic semiconductors



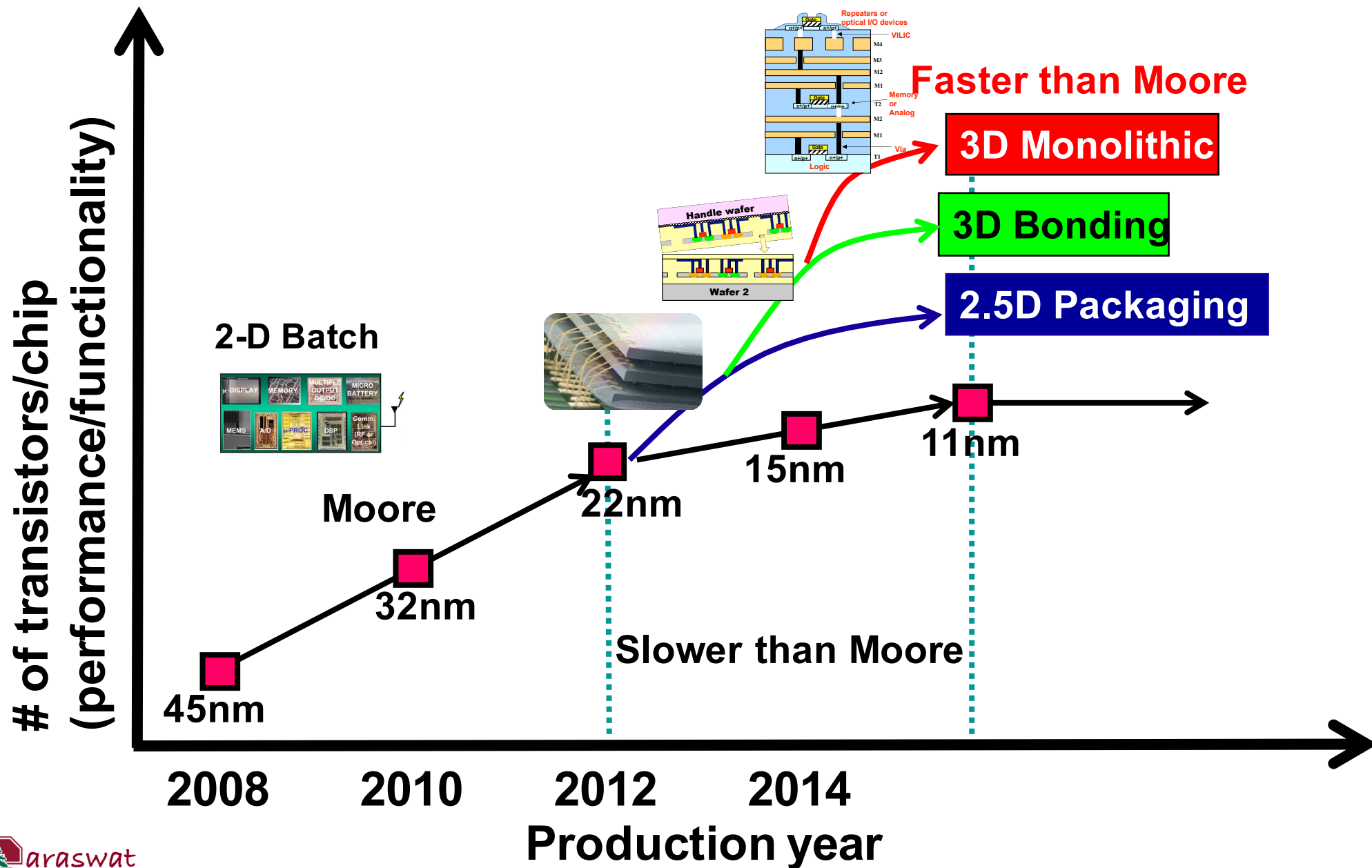


# Monolithic 3D Integration of Si MOSFETs with RRAMs and CNTFETs

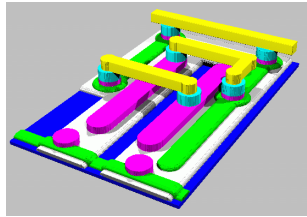


Max Shulaker, et al., IEDM, December 2014,  
VLSI Symp. 2014

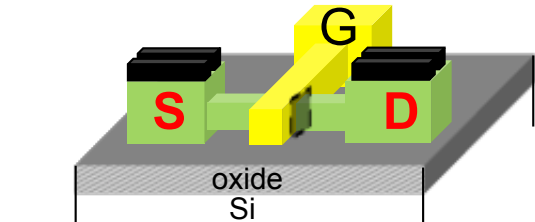
# Heterogeneous 3D Integration Faster than Moore



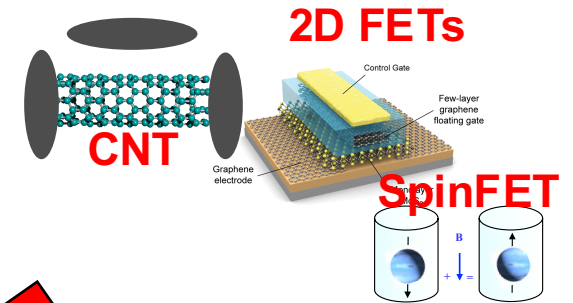
# Future Systems will Require Heterogeneous 3D Integration on a Si Platform



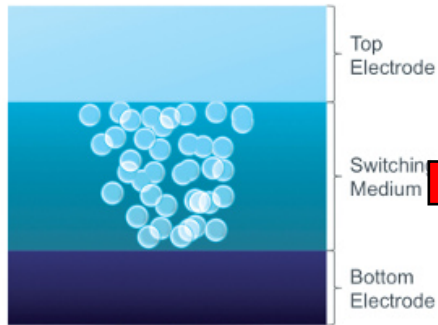
**Metal interconnect**



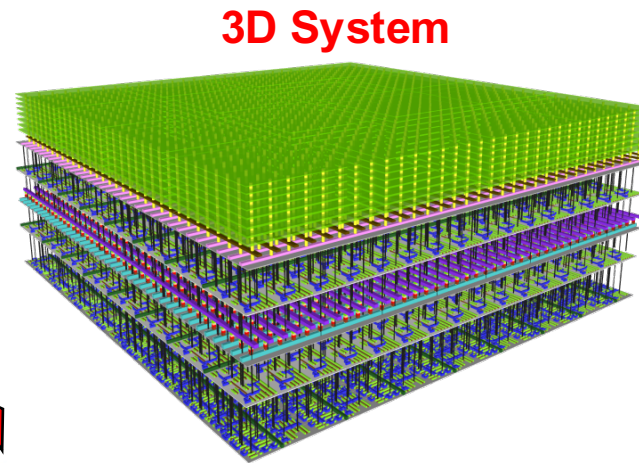
**Conventional transistors**



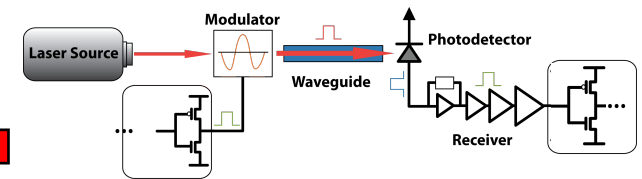
**Novel transistors**



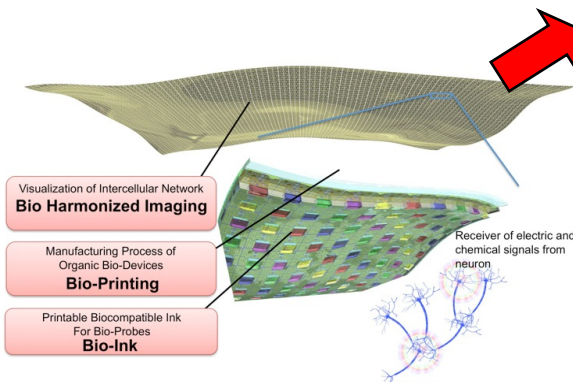
**Memory**



**3D System**

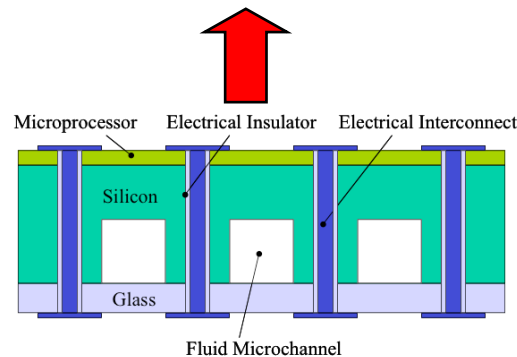


**Photonics**

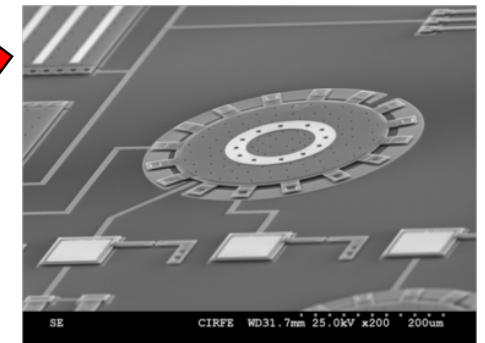


**Clarification of Neuron Network**

**Bio devices**



**Heat Transfer**



**MEMS/Sensors**



# Conclusion

- ☹️ **Cu** resistivity increases as technology scales down. This will be a bottleneck of future high-performance chip.
- 😊 **CNTs** have a significant advantage over Cu wires especially for local interconnects
- 😊 **Optical links** have smallest latency and energy per bit for longer global interconnects requiring higher band width
- 😊 **3D heterogeneous integration** will keep the Moore's law going for awhile.

## Contributors / Collaborators:

Hoyeol Cho, Raj Dutt, Shashank Gupta, Suyog Gupta, Jim Harris, Pawan Kapur, Kyung-Ho Koo, Donguk Nam, Ju Hyung Nam, Ammar Nayfeh, Ali Okay, Jan Petykiewicz, Dave Sukhdeo, Jelena Vuckovic and Hyun-Yong Yu.