Potential Challenges of Metal-Oxide Based Photoresist and Subsequent Rework Removal

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EUV Photo Resist Design Principles

- Small Molecular Building Blocks
- Photocondensed Molecular Metal Oxides
- High EUV Absorbance
- Robust Etch & Mechanical Properties
EUV Photo Resist Development Strategy

Patterning Performance

Fab Integration (Lab-to-Fab)

Working with equipment, materials, consortia, university, and device manufacturer partners
Transition From Lab-to-Fab

- Inpria Y-series photoresists contain organometallic complexes, which are soluble in commonly used fab solvents.

- Demonstrating compatibility with fab equipment and processes is critical for integration in the fab.

- Demonstrate:
  - Zero cross-contamination
  - Film coating and uniformity
  - Film defectivity analysis
  - Metal residue detection on Si backside and EBR region
  - Etch selectivity relative to conventional CAR
  - Ability to rework without surface degradation
    - Particles
    - Metals
Cross-contamination check

Both sides of all monitor wafers analyzed with two techniques:

- TXRF (397 pts)
- VPD-ICP-MS

Experiment schematic:

Monitor wafers, processed through track, PRE-resist install → Coated 50 wafers wafers with Inpria Y-series resist → TXRF (397 pts) → Monitor wafers, processed through track, POST-resist install

Typical fab spec
Coating Metrics – Defectivity

- Defectivity improvement in resist manufacturing
- Comparison between two resists synthesized with standard and improved filtration without POU filter

Improved filtration methods during resist manufacturing helps reduce film defectivity
Coating Metrics – Defectivity

- Defectivity improvement by Coater / Developer
  - Comparison between standard dispense system and FEF (Filtration Enhanced Function) with POU filter

FEF on Coater / Developer system also helps to reduce film defectivity
# Etch Rate Test

## Etch rate comparison under standard Si-ARC/OPL etch condition

<table>
<thead>
<tr>
<th></th>
<th>Conventional CAR resist</th>
<th>Inpria YA series</th>
<th>Inpria YA series with hard bake</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Initial</td>
<td>After etch</td>
<td>Initial</td>
</tr>
<tr>
<td>X-SEM images</td>
<td><img src="image" alt="X-SEM images" /></td>
<td><img src="image" alt="X-SEM images" /></td>
<td><img src="image" alt="X-SEM images" /></td>
</tr>
<tr>
<td>X300k</td>
<td>49 nm</td>
<td>30 nm</td>
<td>15 nm</td>
</tr>
<tr>
<td>PR thickness</td>
<td>49 nm</td>
<td>30 nm</td>
<td>15 nm</td>
</tr>
<tr>
<td>Initial – after</td>
<td>△19 nm</td>
<td>△6 nm</td>
<td>△9 nm</td>
</tr>
</tbody>
</table>

Inpria resist obtained more than 9X higher etch resistance compared to conventional EUV CAR resist under typical Si-ARC / OPL etch condition, same processing time.
TEL ORION™ –hp for Rework

- Unique closed chamber with novel ViPR™ process using SPM + Steam
- Aggressive strip process to remove resist and other organic containing layers with minimum process time & chemical use

<table>
<thead>
<tr>
<th>Challenge</th>
<th>Removal</th>
</tr>
</thead>
<tbody>
<tr>
<td>High dose (&gt;E15) implant DUV</td>
<td>✓</td>
</tr>
<tr>
<td>Tri-layer (Si-ARC up to 43% Si)</td>
<td>✓</td>
</tr>
<tr>
<td>Amorphous C</td>
<td>✓</td>
</tr>
<tr>
<td>Plasma Doped (PLAD)</td>
<td>✓</td>
</tr>
</tbody>
</table>

 waktu

- 1e15 / 2 keV Implanted Resist

- 80%
Rework Test

• Resist strip test with steam injected SPM + SC1
  – Steam Injected SPM time varied; SC1 time fixed

<table>
<thead>
<tr>
<th>Resist component</th>
<th>Method</th>
<th>Detection Limit (E10 atoms/cm²)</th>
<th>Post rework</th>
</tr>
</thead>
<tbody>
<tr>
<td>Metal</td>
<td>TXRF</td>
<td>5</td>
<td>&lt;5</td>
</tr>
</tbody>
</table>

• Inpria resist stripped successfully with steam injected SPM
  – Metal level below detection limit with ≥ 10sec process time
  – Defects at baseline levels with ≥ 20sec process time
Conclusions

- Inpria resist compatibility with CLEAN TRACK™ LITHIUS Pro™ - EUV coater/developer has been demonstrated
- Inpria resist stripped successfully with steam injected SPM
- Metal level below detection limit with ≥ 10sec process time
- Defects at baseline levels with ≥ 20sec process time
Acknowledgements

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Thank you